NXP Semiconductors Application Note

Document Number: AN5260

PBL Configuration using QCVS

1. Introduction

This document describes the steps required to configure pre-boot loader (PBL) on NXP QorIQ platform using the PBL tool included in QorIQ Configuration and Validation Suite (QCVS).

This document explains:

- Purpose of the QCVS PBL tool
- How to configure PBL using the PBL tool
- PBL tool limitations

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2. Preliminary background

The QCVS PBL tool provides you a graphical user interface (GUI) for editing a PBL binary in a decoded form. The PBL binary can be created from scratch or imported from an existing reset configuration word (RCW) memory dump. Such memory dumps can be obtained using U-Boot.

The RCW data contains reset configuration information that PBL loads from a memory device during power-on or hardware reset. All data read from the RCW source is written to the RCW status registers by PBL. If RCW selects pre-boot initialization (PBI), then the PBI commands are processed and routed to CCSR, DDR, and other memory spaces.

The PBL tool operates in the context of documented PBL configuration constraints and errata and prevents the user from violating them. The output of the PBL tool is a PBL binary that can be used to pre-program the platform.

3. Creating a QorIQ configuration project

Perform the following steps to create a QorIQ configuration project with the PBL tool:

- 1. Open the QCVS Eclipse integrated development environment (IDE).
- Choose File > New > QorIQ Configuration Project from the IDE menu bar. The New QorIQ Configuration Project wizard starts, displaying the Create a QorIQ Configuration Project page.
- 3. Specify the project name in the **Project name** text box, and click **Next**. The **Devices** page appears.
- 4. Choose a device and a device version, and click Next. The Toolset selection page appears.
- Select the PBL Preboot Loader RCW configuration checkbox, and click Next. The PBL configuration page appears, where you can choose an initial PBL configuration for your project using one of the following three options, specify other required settings, and complete project creation:
- Create default configuration
- Import configuration from an existing PBL file
- <u>Use RCW Hard-coded configuration</u>

3.1. Create default configuration

The default PBL configuration includes basic settings for RCW and no PBI commands. Use the **Create default configuration** option when neither you need to customize an existing RCW dump (see Import configuration from an existing PBL file) nor you have a hard-coded RCW configuration to work on (see Use RCW Hard-coded configuration).

The figure below shows the **PBL configuration** page with the **Create default configuration** option selected.

PBL Configuration using QCVS Application Note

Creating a QorIQ configuration project

Figure 1. Creating a default configuration

New QorIQ Configuration Project	
PBL configuration	
Choose PBL configuration	
Basic Configuration	
Oreate default configuration	=
Import configuration from an existing PBL file	
Use RCW Hard-coded configuration	
Create default configuration for PBL.	*
	T
	Cancel

3.2. Import configuration from an existing PBL file

The **Import configuration from an existing PBL file** option allows you to import PBL from other projects/resources, such as SDK. This option is useful when you need to quickly investigate and/or customize an existing PBL.

The figure below shows the **PBL configuration** page with the **Import configuration from an existing PBL file** option selected.



Figure 2. Importing a configuration from an existing PBL file

New QorIQ Configuration Project	
PBL configuration	
Choose PBL configuration	
Paris Castinuation	<u>_</u>
© Create default configuration	
Import configuration from an existing PBL file	E
Use RCW Hard-coded configuration	
Import Configuration	
Input file: X:\tftpboot\ls2085ardb\EAR5\PBL_0x2a_0x41_1333.bin	Browse
File format: Binary	-
Select input file to be used for importing an existing PBL configuration and choose th appropriate file format.	ie 🔺
	Cancel

3.3. Use RCW Hard-coded configuration

A hard-coded RCW configuration can be used as the starting point for the PBL configuration. If you are new to the QCVS PBL tool, then you should use the **Use RCW Hard-coded configuration** option to create a QorIQ configuration project with the PBL tool. Hard-coded RCWs have been tested with the QorIQ reference design boards (RDBs) and represent a good starting point to customize a PBL for a custom or reference design board.

The figure below shows the **PBL configuration** page with the **Use RCW Hard-coded configuration** option selected.



New QorIQ Configuration Project	3
PBL configuration	
Choose PBL configuration	
Basic Configuration	1
Create default configuration	-
Import configuration from an existing PBL file	-
Ise RCW Hard-coded configuration	
Hard-coded Configuration	
Hard-coded RCW: 0x9B 🔹	
Choose a hard-coded RCW option as the starting point for the PBL configuration. The processor defines these hard-coded configurations and allows one to be specified with POR signals. Doing so bypasses using the PBL to load in RCW data from a non-volatile memory device. Choosing one of these hard-coded options in this wizard will produce an initial RCW configuration based on the corresponding hard-coded configuration.	
(?) < Back Next > Finish Cancel	•
	J

4. Basic PBL operations

When you create a QorIQ configuration project with the PBL tool, a PBL component is created under the **Components** folder in the **Components** view, as shown in the figure below.





To view or edit the properties of the PBL component, select the PBL component in the **Components** view. The component properties are displayed on the **Properties** page of the **Component Inspector** view, as shown in the figure below.

Figure 5. Component Inspector view

NOTE If the **Component Inspector** view is not open already, then open it by right-clicking a component in the **Components** view and choosing **Inspector** from the shortcut menu.

Name Value Details Device PBL PBL A Reset Configuration Word (RCW) RCW Source Serial NOR A PLL Configuration A A A System PLL A A

A Reset Configuration Word (RCW)		
RCW Source	Serial NOR	
PLL Configuration		
⊿ System PLL		
SYS_PLL_CFG [1-0]	0b00 - For all valid Platform PLL frequencies	
SYS_PLL_RAT [6-2]	0b10010 - 18:1	
Platform Clock	1.499 GHz	
Memory Controller Complex PLL		
DDR Reference Clock	133.000 MHz	
MEM_PLL_CFG [9-8]	0b00 - All valid DDR PLL frequencies	
MEM_PLL_RAT [15-10]	0600100 - 4:1	
DDR1 Data Rate	532.000 MT/s	
MEM2_PLL_CFG [17-16]	0b00 - All valid DDR PLL frequencies	
MEM2_PLL_RAT [23-18]	06001011 - 11:1	
DDR2 Data Rate	1.463 GT/s	
Cluster Groups PLL		
Cluster Group A PLL		
CGA_PLL1_CFG [25-24]	0b00 - All valid cluster group A PLL frequencies	
CGA_PLL1_RAT [31-26]	0b100000 - 32:1 (Async mode)	
Cluster Group A PLL 1 Clock	2.666 GHz	
CGA_PLL2_CFG [33-32]	0b00 - All valid cluster group A PLL frequencies	
CGA_PLL2_RAT [39-34]	0b100000 - 32:1 (Async mode)	
Cluster Group A PLL 2 Clock	2.666 GHz	
Cluster Group B PLL		
CGB_PLL1_CFG [49-48]	0b00 - All valid cluster group B PLL frequencies	
CGB_PLL1_RAT [55-50]	0b100000 - 32:1 (Async mode)	

As you can see in the figure above, the component properties are grouped under various groups and subgroups. All the settings and properties of the PBL component are sorted by the RCW position.

Following are some basic PBL operations you can perform in the Component Inspector view:

- <u>Change RCW bit field values</u>
- Add PBI commands to a PBL image
- Import a PBL configuration from a file
- <u>Generate a PBL image</u>
- <u>Automatic PBL validation</u>
- Synchronize PBL with other IP blocks
- <u>View RCW status registers</u>

•

Basic Advanced

4.1. Change RCW bit field values

For most of the RCW fields, you can change the value by typing in a new value or choosing another value from a menu. For other fields (for example, SerDes protocol options), a more advanced graphical user interface (GUI) is displayed to change the value.

The figure below shows an example of changing a field value by choosing another value from a menu.

Figure 6. Changing a field value by choosing another value from a menu

Name	Value	Details	
MEM2_PLL_SPD [130]	0b0 - High speed operation (vco_d		
CGA_PLL1_SPD [132]	0b0 - High speed operation (vco_d		
CGA_PLL2_SPD [133]	0b0 - High speed operation (vco_d		
CGB_PLL1_SPD [135]	0b0 - High speed operation (vco_d		
CGB_PLL2_SPD [136]	0b0 - High speed operation (vco_d		
Cluster PLL Selection (Bits 175-144)			
Clocking Selection - Hardware Accelerators (Bits 208-176)			
Other Clocking and Clock Domains (Bits 255-209)			
Boot Configuration (Bits 291-256)			
BOOT_LOC [264-260]	0b00000 - PCI-Express 1 (if present		
BOOT_HO [265]	0b1 - All cores in holdoff 🛛 👻		
SB_EN [266]	0b0 - All cores except core X in holdo	ff	
FLASH_MODE [275-267]	0b1 - All cores in holdoff		
PBI_LENGTH [287-276]	L		
SDBGEN [288]	0b0 - Secure debug is not enabled		
Layerscape Chassis Expansion Area (Bits 351-292))			
b Chassis Non-IFC Extension Pin Configuration (Bits 383-352)			
Chassis IFC Base Pin Configuration (Bits 479-448)			
Memory and High Speed I/O Configuration (Bits 511-480)			
SoC Specific Configuration (Bits 895-832)			
SERDES PLL and Protocol Configuration (Bits 911-896)			
Layerscape Chassis EXPANSION AREA (Bits 1023-912)			
N_PRI Data			

The figure below shows an example of changing a field value by using an advanced GUI.

ame	SRDS_PRTCL_S1 [919	-912]							
1588 [832]	SRDS_PRTCL_S1				SERDES1				
USB [833]		н	G	F	E	D	C	В	A
USB3_CLK_FSEL [849-844]	O 00 (0b0000000)	Used by hard-coded value							
SERDES PLL and Protocol Configuration (Bits 9		· · · · · · · · · · · · · · · · · · ·		PFX1	,			PEX2	
SRDS_PLL_PD_PLL1 [896]	O3 (0b0000011)		(8/	5/2.5G)				(8/5/2.5G)	
SRDS_PLL_PD_PLL2 [897]		SGMII1 (MS)	SGMII2 (MS)	SGMIB (MS)	SGMII4 (MS)			PEX2	
SRDS_PLL_PD_PLL3 [898]	0 02 (000000101)	(1.25G)	(1.25G)	(1.25G)	(1.25G)			(8/5/2.5G)	
SRDS_PLL_PD_PLL4 [899]	07 (060000111)	SGMII1 (MS)	SGMII2 (MS)	SGMIB (MS)	SGMII4 (MS)	SGMII5	SGMII6	SGMII7	SGI
▲ Layerscape Chassis EXPANSION AREA (Bits 102)		(1.25G)	(1.25G)	(1.25G)	(1.25G)	(1.25G)	(1.25G)	(1.25G)	(1.2
SRDS_PRTCL_S1 [919-912]	0.09 (0500001001)	SGMII1 (MS)	SGMII2 (MS)	SGMIB (MS)	SGMII4 (MS)	SGMII5	SGMII6	SGMII7	SGI
SRDS_PRTCL_S2 [927-920]	0 05 (050001001)	(3.125G)	(3.125G)	(3.125G)	(3.125G)	(3.125G)	(3.125G)	(3.125G)	(3.1
SRDS_PLL_REF_CLK_SEL_S1_PLL1 [928]	O 0A (0b00001010)	SGMII1 (MS)	SGMII2 (MS)	SGMIB (MS)	SGMII4 (MS)	SGMII5	SGMII6	SGMII7	SGI
SRDS_PLL_REF_CLK_SEL_S1_PLL2 [929]	<u> </u>	(3.125G)	(3.125G)	(3.125G)	(3.125G)	(1.25G)	(1.25G)	(1.25G)	(1.2
SRDS_PLL_REF_CLK_SEL_S2_PLL1 [930]	OC (060001100)	SGMII1 (MS)	SGMII2 (MS)	SGMIB (MS)	SGMII4 (MS)	SGMII5	SGMII6	SGMII7	SG
SRDS_PLL_REF_CLK_SEL_S2_PLL2 [931]		(1.256)	(1.256)	(1.256)	(1.256)	(3.1256)	(3.1256)	(3.1256)	(3.1.
SRDS_DIV_PEX_S1 [945-944]	O 0E (0b00001110)	SGMIII (MS)	SGMII2 (MS)	SGMIB (MS)	SGMII4 (MS)	SGMII5	SGMII6	SGMII7	SG
SRDS_DIV_PEX_S2 [947-946]		(5.1250)	(5.1250)	(1.250)	(1.250)	(1.230)	(1.250)	(1.230)	(1.4
PBI Data	💿 10 (0ь00010000)	(3.125G)	(3.1.25G)	(1.25G)	(1.256)	(3.1256)	(3.125G)	(3.125G)	(3.1
PBL Data		(3.1250)	(5.1250)	(1.250)	(1.250)	(5.1250)	(5.1250)	(5.1250)	[
Offset									
Output Format	See SRDS PRTCL SLO	ptions: 1'0b0000	000 - used by ha	d-coded values 1'	0600000011 - H:E-P	Cle1:D-A:P	CIe2. 1'0b00	000101 - H:E-4xSG	D-A:PC
Checksum in RCW Load command	1'0b00000111 - H:E-4x	G;D-A:4xSG. 1'0	00001001 - H:E-4	xSG;D-A:4xSG. 1'0k	00001010 - H:E-4x5	SG;D-A:4xSC	5.1'0b00001	100 - H:E-4xSG;D-A	A:4xSG.
Additional Binary Data	1'0b00001110 - H:E-4x	5G;D-A:4xSG. 1'0ł	00010000 - H:E-4	xSG;D-A:4xSG. 1'0b	00010010 - H:E-4x5	SG;D-A:4xSO	G. 1'0600010	100 - H:E-4xSG;D-A	A:4xSG.

Figure 7. Changing a field value by using an advanced GUI

4.2. Add PBI commands to a PBL image

You can add the PBI commands to a PBL image by using the **PBI Data input** property under the **PBI Data** group on the **Properties** page of the **Component Inspector** view. Perform the following steps to add the PBI commands:

1. Select the **PBI Data input** property in the **Name** column and click the ellipsis (...) button in the **Value** column, as shown in the figure below.

Figure 8. Setting PBI Data input property

⊿ PBI Data	
PBI Data input	(click here and press [] button)
CRC in final Stop command	yes
Offset	0
Output Format	Binary
Checksum in RCW Load command	yes
Additional Binary Data	(click here and press [] button)

The PBI Data input editor opens, as shown in the figure below.

Figure 9. PBI Data input editor

Properties Import			
Name	*	PBI Data input	
USB3_CLK_FSEL [849-844]		Select PBI command CCSR Write	
SERDES PLL and Protocol Configuration (Bits 9		Command assumption	
SRDS_PLL_PD_PLL1 [896]			
SRDS_PLL_PD_PLL2 [897]		SYS_ADDR (0x) 1000000	
SRDS_PLL_PD_PLL3 [898]		CCSR DATA (0x) 0000000	
SRDS_PLL_PD_PLL4 [899]			
Layerscape Chassis EXPANSION AREA (Bits 102)		Byte Count 4 🗸	
SRDS_PRTCL_S1 [919-912]			
SRDS_PRTCL_S2 [927-920]		- Add Command	
SRDS_PLL_REF_CLK_SEL_S1_PLL1 [928]			_
SRDS_PLL_REF_CLK_SEL_S1_PLL2 [929]		Added PBI Commands:	010
SRDS_PLL_REF_CLK_SEL_S2_PLL1 [930]			
SRDS_PLL_REF_CLK_SEL_S2_PLL2 [931]			
SRDS_DIV_PEX_S1 [945-944]			
SRDS_DIV_PEX_S2 [947-946]			
⊿ PBI Data			
PBI Data input			
CRC in final Stop command		Restore Apply	
▲ PBL Data			
Offset	=	Use this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode.	
Output Format		Version specific item: Settings supported only for devices using Reset Configuration Word (RCW).	
Checksum in RCW Load command			
Additional Binary Data	-		
			1

2. Choose the appropriate PBI command from the **Select PBI command** menu, as shown in the figure below.

Figure 10. Choosing a PBI command

PBI Data input							
Select PBI command	CCSR Write	•					
Command parame	ters CCSR Write AltConfig Write						
SYS_ADDR (0x)	0(Block Copy						
CCSR_DATA (0x)	0 Load Condition						
Byte Count	4 Load Security Header Load Boot 1 CSF Header Pointer						
	Poll (short) Poll (long) Wait	Modify Command					
Added PBI Comman	ds: Jump Jump Conditional Stop		×	*	ر ا	ŀ 🗹	<u></u>

3. Edit command parameters in the **Command parameters** group and click the **Add Command** button. The PBI command is added in the **Added PBI Commands** pane, as shown in the figure below.

Figure 11. Editing a PBI command

PBI Data input									
Select PBI command	CCSR Write	e	•						
Command parameter	rs	_							
SYS_ADDR (0x) 1	11E214								
CCSR_DATA (0x) 1	12345678								
Byte Count 4	• •								
		·							
		🕂 Add Command	Modify Command						
Added PBI Commands:				×	*	企	Ŷ	-0	01
CCSR 4-byte Write to 0	0x0011e214, c	data=0x12345678							

You can view the PBI commands in two modes: disassembly view and raw data view. To switch between the two modes, click the rightmost button on the toolbar of the **Added PBI Commands** pane, as shown in the following figures.

Figure 12. Disassembly view

Added PBI Commands:	×	*	Û	Ŷ	1 🗟	l
CCSR 4-byte Write to 0x0011e214, data=0x12345678						

Figure 13. Raw data view

Added PBI Commands:	010
3011E21412345678	*

4. Click the Apply button to add the PBI commands to the PBL image.

Select PBI command CCSR Write Command parameters SYS_ADDR (0x) 11E214 CCSR_DATA (0x) 12345678 Byte Count 4 CCSR_DATA (0x) 12345678 Byte Count 4 CCSR_delta Command CCSR_delta Commands CC									
Command parameters SYS_ADDR (0x) 11E214 CCSR_DATA (0x) 12345678 Byte Count 4 Add Command Image: Modify Command Add Command Image: Modify Command Add Command Image: Modify Command Image: Commands Image: Comments (#) can be added in Raw mode. Image: Image: Comments (#) can be added in Raw mode. Image: Image: Comments (#) can be added in Raw mode.	Select PBI command	CCSR Write		•					
SYS_ADDR (0x) 11E214 CCSR_DATA (0x) 12345678 Byte Count 4 Add Command Modify Command Added PBI Commands: CCSR 4-byte Write to 0x0011e214, data=0x12345678 Restore Apply Ase this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. 'ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	Command parameter	ers							
CCSR_DATA (0x) 12345678 Byte Count Add Command Modify Command Added PBI Commands: CCSR 4-byte Write to 0x0011e214, data=0x12345678 Restore Apply Ase this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. 'ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	SYS_ADDR (0x)	11E214							
Byte Count 4 - Add Command Modify Command Added PBI Commands: X X X V V CCSR 4-byte Write to 0x0011e214, data=0x12345678 Restore Apply Ase this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. I'resion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	CCSR_DATA (0x)	12345678							
Added PBI Commands: CCSR 4-byte Write to 0x0011 e214, data=0x12345678 Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. 'ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	Byte Count	4 👻							
Added PBI Commands: CCSR 4-byte Write to 0x0011e214, data=0x12345678 Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. 'ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).			4 Add Command	Modify Command	d				
CCSR 4-byte Write to 0x0011e214, data=0x12345678 Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	Added PBI Command	s:				56	企	Л	
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	CCSR 4-byte Write to	0.0044.044.1.							
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	econtri byte mite to	0x0011e214, dat	a=0x12345678						
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	cost + byte mile to	0x0011e214, dat	a=0x12345678						
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	econtrojte inite to	0x0011e214, dat	a=0x12345678						
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).		0x0011e214, dat	a=0x12345678						
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	Controj termeto	0x0011e214, dat	a=0x12345678						
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).		0x0011e214, dat.	a=0x12345678						
Restore Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).		0x0011e214, dat	a=0x12345678						
Apply Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).		0x0011e214, dat	a=0x12345678						
Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).		0x0011e214, dat	a=0x12345678						
Jse this property to add PBI commands to the PBL image. Comments (#) can be added in Raw mode. /ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	Restore	0x0011e214, dat	a=0x12345678						
/ersion specific item: Settings supported only for devices using Reset Configuration Word (RCW).	Restore	0x0011e214, dat	a=0x12345678						
	Restore Apply Use this property to ac	d PBI command	a=0x12345678 Is to the PBL image. Co	omments (#) can be adde	d in Raw mode.				
	Restore Apply Use this property to ac Version specific item:	date date date date date date date date	a=0x12345678 Is to the PBL image. Co ed only for devices usi	o mments (#) can be adde ng Reset Configuration W	d in Raw mode. /ord (RCW).				
	Restore Apply Use this property to ac Version specific item: 1	date of the second seco	a=0x12345678 Is to the PBL image. Co ed only for devices usin	omments (#) can be adde ng Reset Configuration W	d in Raw mode. /ord (RCW).				
	Restore Apply Use this property to ac Version specific item: 1	date of the second seco	a=0x12345678 Is to the PBL image. Co ed only for devices usi	omments (#) can be adde ng Reset Configuration W	d in Raw mode. /ord (RCW).				
	Restore Apply Use this property to ac Version specific item:	date of the second seco	a=0x12345678 Is to the PBL image. Co ed only for devices usi	omments (#) can be adde ng Reset Configuration W	d in Raw mode. /ord (RCW).				

Figure 14. Adding PBI commands to a PBL image



4.3. Import a PBL configuration from a file

To import a PBL configuration for an existing PBL component, perform these steps:

- 1. Click the Import tab in the Component Inspector view. The Import page appears.
- 2. Choose a PBL file by clicking the **Load from file** button. The file format of the chosen file is detected automatically and its content is displayed in the Rich Text Format in an editor available in the **Input data** group, as shown in the figure below.

Figure 15. Loading a PBL file

📎 Componen	t Inspe	ctor	- PBL	53	٩	Con	npon	ents	Libr	ary								Ba	sic Advanced	*	~ - [3
Properties Im	port																					
Choose a file.	Its cor	ntent	s and	l for	mat	will b	e ins	erted	l into	o the	inpu	it are	a be	low.								
L and from fi	le le		June							, and	mpe											
Load from fi	IC																					
Input data																						
Format:	xxd Ol	bject	Dum	ър					•	-												
Endianness:	Little	Endia	in 🖣	•																		
00000000	: 55	aa	55	aa	00	00	10	80	30	28	28	40	40	00	40	40	U.U0((00.00				*	
00000010	: 00	00	00	00	00	00	00	00	00	00	00	00	00	00	20	00						
00000020	: 00	00	20	00	00	00	00	00	80	29	c1	00	80	25	00	00)§					
00000030	: 00	00	00	00	00	00	00	00	0b	0e	00	00	00	00	00	00						
00000040	: 00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
00000050	: 00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
00000060	: 00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00						
00000070	: 00	70	02	00	00	00	00	00	00	00	2a	41	00	00	00	00	.p*A					
00000080	: 00	00	00	00	00	00	00	00	d0	91	İb	ec	04	04	e0	30						
00000090	: 00	00	00	00	00	04	eu	30	00	00	10	30	00	00	08	33						
0000000000	: 00	00	00	-00	00	05	08	33	a/ 4=	20	00	67	20	06	eu	30						
000000000	: 00	00	00	au	00	00	BI	80	41	38	eī	6/					08.g					
4																						
																_					,	
																In	nport					

- 3. Edit the PBL file in the editor, as needed.
- 4. Click the Import button to import the new PBL configuration.
- 5. Switch to the **Properties** tab to view or edit the imported PBL configuration.

Using the steps provided in this section, you can import files having the following file formats:

- XXD Object Dump
- S-record
- U-Boot Flash Dump
- Hex String
- U-Boot CCRS Startup Dump (RCW only)
- CW JTAG Config (RCW only)
- Hex String (RCW only)
- Test Table (RCW only)

NOTE By default, the import operation tries to convert the memory dump into the XXD Object Dump format and displays it in the Rich Text Format.

4.4. Generate a PBL image

To generate a PBL image from the PBL configuration, perform these steps:

- 1. Select the **Output Format** property under the **PBL Data** group in the **Name** column on the **Properties** page of the **Component Inspector** view.
- 2. Click the corresponding cell in the Value column and choose a file format for the PBL image.

Figure 16. Choosing a file format for PBL file

🛛 Prop	erties Import			
Name		Value	Details	A
	USB3_CLK_FSEL [849-8	0b100111 - 100 MHz.		
4	SERDES PLL and Protoco			
	SRDS_PLL_PD_PLL1 [89	0b1 - PLL is powered down.		
	SRDS_PLL_PD_PLL2 [89	0b1 - PLL is powered down.		
	SRDS_PLL_PD_PLL3 [89	0b1 - PLL is powered down.		
	SRDS_PLL_PD_PLL4 [89	0b1 - PLL is powered down.		
4	Layerscape Chassis EXPA			
	SRDS_PRTCL_S1 [919-9	0b00000011 - H:E-PCle1;D-A:PCle2.		
	SRDS_PRTCL_S2 [927-9	0b00000111 - A-H:8xSG.		
	SRDS_PLL_REF_CLK_SE	0b0 - 100 / 125 / 156.25 MHz.		
	SRDS_PLL_REF_CLK_SE	0b0 - 100 / 125 / 156.25 MHz.		
	SRDS_PLL_REF_CLK_SE	0b0 - 100 / 125 / 156.25 MHz.		
	SRDS_PLL_REF_CLK_SE	0b0 - 100 / 125 / 156.25 MHz.		
	SRDS_DIV_PEX_S1 [945	0b00 - Can train up to a max rate o		
	SRDS_DIV_PEX_S2 [947	0b00 - Can train up to a max rate o		
⊿	PBI Data			
	PBI Data input	(click here and press [] button)		
	CRC in final Stop comma	yes		
⊿	PBL Data			
	Offset	0 <u>H</u>		=
	Output Format	Binary -		
	Checksum in RCW Load o	Binary		
	Additional Binary Data	xxd Object Dump Screcord		-
		U-Boot Commands		
		Hex String		
		CW JTAG Config (RCW only)		
		Hex String (RCW only)		
		Text Table (KCW only)		

3. Click the Generate Processor Expert Code icon in the Components view to generate the PBL image.

Basic PBL operations

Figure 17. Generating PBL image



Using the steps provided in this section, you can generate PBL images with the following file formats:

- Binary
- XXD Object Dump
- S-record
- U-Boot Commands
- Hex String
- CW JTAG Config (RCW only)
- Hex String (RCW only)
- Text Table (RCW only)

4.5. Automatic PBL validation

Each time you change the PBL configuration, the PBL tool performs a check against known constraints and issues. If the configuration is found invalid, then the error or warning messages are displayed for the problematic RCW fields on the **Properties** page in the **Component Inspector** view, as shown in the figure below.

Figure 18. PBL validation

3 Properties Import									
Name	Value	Details	*						
Device	PBL	PBL							
🔺 🌹 Reset Configuration Word (
RCW Source	Serial NOR		=						
PLL Configuration									
System PLL									
SYS_PLL_CFG [1-0]]	Custom value can be used only if "Ignore Constraints and non-Critical Errors" option is turned ON							
SYS_PLL_RAT [6-2]] 0Ь10010 - 18:1								
Platform Clock	1.499 GHz								
⊿ Memory Controller C									
DDR Reference Clo	100.000 MHz								
MEM_PLL_CFG [9-	0b00 - All valid DDR PLL frequencies								
MEM_PLL_RAT [15	0b000110 - 6:1								
DDR1 Data Rate	600.000 MT/s								
MEM2_PLL_CFG [1	0b00 - All valid DDR PLL frequencies								
MEM2_PLL_RAT [2	06000110 - 6:1								
DDR2 Data Rate	600.000 MT/s								
⊿ Cluster Groups PLL									
⊿ Cluster Group A F									
CGA_PLL1_CFC	0b00 - All valid cluster group A PL								
CGA_PLL1_RAT	0b100000 - 32:1 (Async mode)								
Cluster Group	2.666 GHz								
CGA_PLL2_CFC	0b00 - All valid cluster group A PL								
CGA_PLL2_RA	0b100000 - 32:1 (Async mode)								
Cluster Group	2 666 GH7		Ψ.						

The error or warning messages are also displayed with additional details in the **Problems** view, as shown in the figure below.

Figure 19. Problems view

🔐 Problems 🕴			1	
1 error, 0 warnings, 0 others				
Description	Resource	Path	Location	Туре
a 📀 Errors (1 item)				
😣 Custom value can be used only if "Ignore Constraints and non-Critical Errors" option is turned ON (SYS_PLL_CFG [1-0])	ls2080		PBL/SYS_PLL	Processor Exp

4.6. Synchronize PBL with other IP blocks

You can synchronize the PBL component with other intellectual property (IP) blocks, such as SerDes or DDR, if the corresponding component is available in the current project.

To synchronize the PBL component with a SerDes component, perform these steps:

- 1. Ensure that a SerDes block component is available in the current project.
- 2. Double-click a SerDes component grouped under the SerDes block component in the **Components** view. The properties of the SerDes component are displayed on the **SerDes Configuration and Validation** page in the **Component Inspector** view.
- 3. Click the **Apply the configuration to PBL component** button at the top-left corner (second button) of the **SerDes Configuration and Validation** page to synchronize the PBL component with the SerDes component, as shown in the figure below.

SerDes Cor	nfiguration a	nd Validatio	1												
8 🕹															
DLL	Lane H Lane G Lane F Lane E Lane D Lane C						Lar	ne B	•						
PLL	SD1_Tx0	SD1_Rx0	SD1_Tx1	SD1_Rx1	SD1_Tx2	SD1_Rx2	SD1_Tx3	SD1_Rx3	SD1_Tx4	SD1_Rx4	SD1_Tx5	SD1_Rx5	SD1_Tx6	SD1_Rx6	٤
	PC	le1	XF	-12	XF	в	X	-14	PC	Ie2	XF	-16	X	F17	=
	(2	5)	(10.3	3125)	(10.3	3125)	(10.:	3125)	(2	.5)	(10.3	3125)	(10.:	3125)	
										-				-	H
		~	~	~	~		~	~	~	~	~	~			-
•	4														
Lane H Co	onfiguration	Validation													
V Set a	as first lane														
Trans	mitter				Receiver										
					neccirci			_							Ξ
Outp	ad Ctrl E	nabled	•		Rx Termina	ition Termi	ination to svs	is i			💌 Equ	alization			
📃 In	vert data				🔲 Invert da	ata					🗸 Bo	ost			
– E	qualization				▼ Electri	cal idle					Gair	nk2			-
							1.1.00				Sou	rce Use rxea	adaption d	erived gaink2	Ē
Ту	pe	2 Lei	/els	-	Ihreshol	d Disat	ble LOS		•	_					-
Pre	Cursor sign	0	•		Enter idle	e filter Bypa	ss Unexpecte	ed Entrance i	nto Idle	•	Valu	ie 0 🔻			
PreCursor ratio No equalization Exit idle filter Force Exit AFTER Min Time in Idle Data stopped Gaink3															
•							III							4	

Figure 20. Synchronizing PBL and SerDes components

4. Select the PBL component in the **Components** view and verify the SerDes fields on the **Properties** page of the **Component Inspector** view, as shown in the figure below.

Figure 21. Verifying SerDes fields of PBL component

Properties Import			
Name	Value	Details	*
HOST_AGENT_PEX1 [485]	0b1 - Agent mode.		
HOST_AGENT_PEX2 [486]	0b0 - Host mode.		
HOST_AGENT_PEX3 [487]	0b0 - Host mode.		
HOST_AGENT_PEX4 [488]	0b0 - Host mode.		
SoC Specific Configuration	n		
1588 [832]	0b1 - IEEE 1588.		
USB [833]	0b1 - {GPIO4[24:27]}.		
USB3_CLK_FSEL [849-844]	0b100111 - 100 MHz.		
▲ SERDES PLL and Protocol Co			
SRDS_PLL_PD_PLL1 [896]	0b0 - PLL is not powered down.		
SRDS_PLL_PD_PLL2 [897]	0b0 - PLL is not powered down.		
SRDS_PLL_PD_PLL3 [898]	0b0 - PLL is not powered down.		
SRDS_PLL_PD_PLL4 [899]	0b0 - PLL is not powered down.		
⊿ Layerscape Chassis EXPANSI	0		
SRDS_PRTCL_S1 [919-912]] 0b00111011 - H:E-PCIe1,3xXFI;D-A:		
SRDS_PRTCL_S2 [927-920]] 0b01001001 - A:D-4xSG;E:H:PCIe4,		
SRDS_PLL_REF_CLK_SEL_S	2 0b0 - 100 / 125 / 156.25 MHz.		
SRDS_PLL_REF_CLK_SEL_S	3 0b0 - 100 / 125 / 156.25 MHz.		
SRDS_PLL_REF_CLK_SEL_S	х 0ь0 - 100 / 125 / 156.25 MHz.		E
SRDS_PLL_REF_CLK_SEL_S	. 0b0 - 100 / 125 / 156.25 MHz.		
SRDS_DIV_PEX_S1 [945-94	4 0b10 - Can train up to a max rate o		
SRDS_DIV_PEX_S2 [947-94	6 0b10 - Can train up to a max rate o		
⊿ PBI Data			
DRI Data input	(click here and press [] hutton)		•

4.7. View RCW status registers

To have an overview of the RCW status registers, perform these steps:

- 1. Choose **Window > Show View > Other** from the IDE menu bar. The **Show View** dialog appears.
- 2. Choose **Processor Expert > Configuration Registers** and click **OK**. The **Show View** dialog closes and the **Configuration Registers** view appears, displaying the details of the RCW status registers, as shown in the figure below.



The **Configuration Registers** view reflects any changes made in the PBL configuration. Note that the don't care bits are displayed using the "?" character.

Basic PBL operations

Advanced PBL operations

5. Advanced PBL operations

This section is divided into the following subsections:

- Force RCW bit fields
- Add additional payload to a PBL image
- Errata support
- Endianness aspects

5.1. Force RCW bit fields

You can make an RCW bit field have a value that is not supported in the PBL tool, by default. Follow these steps to force an RCW bit field to have unsupported value:

1. Click the **View Menu** button (down arrow button) on the toolbar of the **Component Inspector** view and choose **Ignore Constraints and non-Critical Errors**, as shown in the figure below.

Figure 23. Ignoring constraints and non-critical errors

🗞 *Component Inspector - PBL 🛛	🗞 Components Library				Basic Advanced 🎽 🏾 🗖 🗖			
Properties Import				A	Search Ctrl+F			
Name	Value	Details			Basic			
Device	PBL	PBL			Advanced			
Reset Configuration Word (RCV)	N							
RCW Source	Serial NOR			\checkmark	Ignore Constraints and non-Critical Errors			
PLL Configuration					Executed All			
⊿ System PLL					Expand All			
SYS_PLL_CFG [1-0]	0b00 - For all valid Platform PLL fr				Collapse All Help on Component			
SYS_PLL_RAT [6-2]	0ь10010 - 18:1							
Platform Clock	1.499 GHz				Save Component Settings as Template			
Memory Controller Com					Edit comment			
DDR Reference Clock				Luc comment				
MEM_PLL_CFG [9-8]	0b00 - All valid DDR PLL frequencies			Open New Pinned View				
MEM_PLL_RAT [15-10] 0ь000110 - 6:1							
DDR1 Data Rate	600.000 MT/s				Tabs view			

- 2. Select an RCW bit field on the **Properties** page.
- 3. Select the **Custom Bitfield Value** option and specify a custom value for the RCW bit field, as shown in the figure below.



Figure 24. Specifying a custom RCW bit field value



4. Click Apply. The new value is added to the PBL configuration.

5.2. Add additional payload to a PBL image

You can add to a PBL image additional binary payload, such as U-Boot. This is useful to create boot images for the SPI/SD/NAND flash when PBL can be edited without decoupling it from the U-Boot binary. At code generation, the binary payload is automatically re-attached to the modified PBL.

To add additional binary data to the PBL image, perform these steps:

- 1. Select the Additional Binary Data property under the PBL Data group in the Name column on the Properties page of the Component Inspector view.
- 2. Click the ellipsis (...) button in the Value column. The Additional Binary Data editor opens.
- 3. Specify a binary file to be added to the PBL image, in the Location field of the Specify file group.
- 4. Specify the offset and placement for the binary payload in the **Placement** group, as shown in the figure below.

Advanced PBL operations

Figure 25. Additional Binary Data editor

Properties Import	
Name	Additional Binary Data
▲ SerDes 1 Reference Clocks	Specify file
SD1_REF_CLK1 [MHz]	
SD1_REF_CLK2 [MHz]	
SerDes Protocol Selection	
SRDS_PRTCL_S1 [128-135]	workspace File System Variables
SRDS_PLL_REF_CLK_SEL_S1 [160-161]	Placement
USB3_REFCLK_SEL [164-165]	Offset: 0x 300
HDLC1_MODE [166]	
HDLC2_MODE [167]	Relative to RCW/PBI structure: 🔘 beginning 🔘 end
SRDS_PLL_PD_S1 [168-169]	
SRDS_DIV_PEX [176-177]	
USB3_CLK_FSEL [178-183]	
Misc. PLL-Related Configuration	
Boot Configuration	
Clocking Configuration	
Memory and High-Speed I/O Configuration	
General Purpose Information	Restore Apply
Pin Multiplexing Configuration	
Group A Pin Configuration	Add arbitrary binary data after the formal RCW/PBI structure.
Group B Pin Configuration	Version specific item: Settings supported only for devices using Reset Configuration Word (RCW).
SoC-Specific Configuration	
PBI Data	
▲ PBL Data	
Offset	
Output Format	
Additional Binary Data	• •

5. Click **Apply** to apply the changes.

5.3. Errata support

The PBL tool handles errata in the following two ways:

- If the PBL tool can implement the workaround for the erratum impacting the current PBL configuration, then the tool automatically implements the erratum workaround, without notifying the user. Examples of such errata include:
 - An RCW bit field option may not be available anymore
 - A chosen RCW bit field option may translate into a different value (as specified by the errata document of the chosen system-on-chip (SoC)) in the generated PBL binary
- If the PBL tool cannot implement the workaround for the erratum impacting the current PBL configuration, then the tool displays a warning message with the details of the erratum. An example is an erratum that depends on the conditions that cannot be determined by only assessing the PBL configuration (such as, operating temperature, dual inline package (DIP) switch configuration). For such an erratum, the user needs to manually implement the erratum workaround.

Advanced PBL operations

The warning message is displayed for the problematic field on the **Properties** page in the **Component Inspector** view and also in the **Problems** view, as shown in the following figures.

Figure 26. Warning displayed in Component Inspector view

Chassis IFC Base Pin Configuration (Bits 479-		
IFC_GRP_A_BASE [449-448]	0b01 - GPIO[5:3]	
IFC_GRP_D_BASE [455-454]	0b10 - 5 pins GPIO	
IFC_GRP_E_BASE [457-456]	0b01 - {IFC_RB_B[1], IFC_CS_B[1:3], GPIO2[15],	
IFC_GRP_FGHI_BASE [459-458]	0b01 - IFC_AD[15:0] pins function as IFC. IFC	Warning: Erratum A-008460: IFC_A[8:6] may not be
IFC_A_8_6 [460]	0b1 - {IFC_WP_B[3:1]}	
QSPI_OCT_EN [461]	0b1 - 8-bit QuadSPI "A" interface supported, t	

Figure 27. Warning displayed in Problems view

Problems 23			1	
0 errors, 1 warning, 0 others				
Description	Resource	Path	Location	Туре
a 🚯 Warnings (1 item)				
A Warning: Erratum A-008460: IFC_A[8:6] may not be used for GPIO pins when IFC is the source of RCW. (IFC_GRP_FGHI_BASE [459-458])	ls2080		PBL/IFC_GRP	Processor Exp

5.4. Endianness aspects

When you import data in the XXD Object Dump format, you can specify the endianness of the data. However, specifying the endianness is only useful when the data is organized into multibyte words. The endianness option is automatically set to the endianness of the chosen SoC, for example, little endian for the ARMv8-based SoCs.

PBL tool limitations

6. PBL tool limitations

The PBL tool has some known limitations related to:

- <u>Reserved bits</u>
- <u>PBI commands</u>

6.1. Reserved bits

When generating a PBL image, the PBL tool uses the default values of the bits that are marked as *Reserved* in the SoC reference manual. Due to this limitation, some mismatches may occur between the imported PBL image and generated PBL image.

6.2. PBI commands

If the current PBL configuration has PBI commands defined and you import a new PBL image that does not have PBI commands, then the PBI commands are not preserved and you need to manually add them for the new PBL configuration.

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