7/15/98

Errata to

MC68SC302 Passive ISDN Protocol Engine User's Manual

This errata describes corrections to the *MCSC302 Passive ISDN Protocol Engine User's Manual* (MC68SC302UM/AD). For convenience, the section number and page number of the errata item in the user's manual are provided. The **section and page** numbers of **new errata** entries are boldfaced.

Section/Page	Changes

Global	Programming Advisory—Soft Reset.
	
	To perform a soft reset on the SC302, first disable access to the serial EEPROM and then re-enable access by clearing and then setting the SCP enable bit, SPMODE[EN]. The actual reset can then be performed through the command register by setting CR[RST] (and CR[FLG]). Note that the software should wait for the CP to clear CR[FLG] before assuming the soft reset has been completed.
	
	Assuming 0xFFF0 is the address port and 0xFFF2 is the data port, the following code implements the advisory.
	
	ouportw(0xFFF0,0x08B0); // Address of SCP mode register
	ouportw(0xFFF2,0x1400); // Disable SCP
	ouportw(0xFFF2,0x1500); // Enable SCP
	ouportw(0xFFF0,0x0860); // Address of CR register
	ouportw(0xFFF2,0x8100); // Soft reset

4.2, 4-2	Add the following note concerning the reset bit of the command register CR[RST]: ‘The software must wait a minimum of 2ms after setting CR[RST] before the SC302 will respond to ISA or PCMCIA accesses; that is, the software should wait for the CP to clear CR[FLG].’
4.4.2, 4-14	Change the last sentence of the paragraph describing SIMASK to read: ‘Note that the serial data strobes, SDS1 and SDS2, are asserted for the bits set in the associated B-channel mask, and negated for the bits cleared in the SIMASK register.’
5.4.1, 5-7	Change Table 5-3 to read:

Table 5-3. Resource Data Layout

Address	Name	Register-Destination
0x00–01	Serial EEPROM Type/Mode	—
0x02–03	Reserved—must be cleared.	—
0x04	Serial EEPROM Type	—
0x05–06	Reserved—must be cleared.	—
0x07	Implementation-specific information	0x22
0x08	First byte of Standard Resource Data	—

Section/Page	Changes
5.4.1, 5-9	In Figure 5-5, move the words ‘Serial Number’ (originally next to ‘Byte 3’) down one row to align with ‘Byte 0’.
5.4.3, 5-10	Clarify the I/O configuration programming as follows: Byte 0—I/O port descriptor tag. (value = 0b0100_0111 = 0x47) Byte 1—Information byte. The SC302 supports 16-bit decoding, therefore bit 0 = 1, and the reserved bits 7–1 = 0. (value = 0x01)
5.4.4, 5-11	Change the memory configuration programming as follows: Byte 0—Memory range descriptor tag (value = 0b1000_0001 = 0x81) Bytes 1–2—Length of the memory range descriptor. Bits 7–0 = 0x09 and bits 15–8 = 0x00, giving a length of 0x0009. Byte 3—Information field. [Reserved]_[Not ExpansionROM]_[Not shadowable]_[8/16-bit supported]_[Decode support Range Length]_[Non-cachable]_[Writable] (value = 0b0_0_0_1_0_0_0_1 = 0x11)
5.5, 5-17	Change the note directly under the ISI register to read: ‘Loaded from 0x07 in the byte serial device’
5.5, 5-19	At the top of the page, add a closing parenthesis—(Vendor Defined).
5.7, 5-21	The descriptions of IMRNGH and IMRNGL has changed; see errata for 6.6.2, 6-14 below.
6.4.5, 6-6	In Table 6-1, exchange the places of IMRNGH and IMRNGL.
6.6.1, 6-9	In the description of the configuration option register’s interrupt mode bit, COR[LEVIREQ], add the following note: ‘The software must set COR[LEVIREQ] since the SC302 supports only level interrupts.’
6.6.1, 6-10	Change ‘Intr’ to read ‘INTR’.
6.6.2, 6-12	Correct the attribute address of the ACTIVE register to $2000060.
6.6.2, 6-13	In the desription of ACTIVE[ACTV]—Active Bit, change all references of ‘ISA’ to ‘PCMCIA’.

Section/Page	Changes
6.6.2, 6-14	Replace the descriptions of IMRNGH and IMRNGL with the following. Note the attribute address changes.

IMRNGH Attribute address $2000086

7	6	5	4	3	2	1	0
RL[23]=RL[12]	RL[22]=RL[12]	RL[21]=RL[12]	RL[20]=RL[12]	RL[19]=RL[12]	RL[18]=RL[12]	RL[17]=RL[12]	RL[16]=RL[12]
0	0	0	0	0	0	0	0

IMRNGL Attribute address $2000088

7	6	5	4	3	2	1	0
RL[15]=RL[12]	RL[14]=RL[12]	RL[13]=RL[12]	RL[12]	RL[11]=0	RL[10]=0	RL[9]=0	RL[8]=0
0	0	0	0	0	0	0	0

The registers are active in the configuration state.

RL23–RL8 — Range length.

RL23–RL8 corresponds to bit 23 through bit 8 of the upper limit of memory range. Bit7–bit 0 are always zero. RL11–RL8 and RL23–RL13 of the range length are read only. RL12 is read/write and used as an enable bit for the internal memory range.

RL12

1 = Internal memory (4 Kbyte) is enabled. On reads from the range length, the returned value indicates a 4-Kbyte memory range (even if a larger value was written by the software).

0 = Internal memory (4 Kbyte) is disabled; I/O accesses to the internal space are possible if the related I/O base address is not 0. On reads from the range length, 0 is returned.

NOTES:

The memory range length is defined as a mask of address bit23–bit8. If a mask bit is set, the corresponding bit in the address is used in a comparator for address matching.
For PCMCIA operation, mask the internal 4-KB address space (IMRNGH=0xFF, IMRNGL=0xF0) and set ACTIVE[ACTV].
The memory upper limit is defined as being one byte greater than the memory resource assigned.

6.6.2, 6-13 PCMCIA access to the Communication Controller Registers (CCR) in serial EEPROM mode:

In serial EEPROM mode, the CCRs can only be accessed via common memory mode accesses instead of attribute memory accesses as indicated in the manual in section 6.4.2. In fact, all areas of the CCMR

(include DPR and the CCR) can be accessed with common memory accesses (asserting A25). Figure 6-3 should be disregarded and Figure 6-4 used instead (the CIS will still reside in the first locations of DPR).

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