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Typical Endurance for
Nonvolatile Memory



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Introduction

This document explains how Motorola defines typical endurance in the product specification of nonvolatile memory (NVM).

Definition

Endurance refers to the ability of a memory bit to withstand the repeated operation of program/erase (P/E) events and still meet the performance for program and erase time.

Motorola guarantees a minimum endurance in its product specification. In practice, the technology is capable of producing much greater endurance than the specified minimum. To give a better representation of the endurance that can be achieved under nominal conditions¹, Motorola also provides a typical value in the product specification.

Motorola defines typical endurance as the number of P/E cycles that most parts can achieve without failure. It is evaluated by stressing an industry standard sample size^{2,3} at room temperature until intrinsic wear out is observed or until extensive margin to the endurance specification has been achieved.

Example

- Cycle to 500 k. Failures starting @ 356 k → Typical Endurance > 350 k
- Cycle to 500 k. No fail @ 500 k → Typical Endurance > 500 k

1. Nominal conditions = room temperature, nominal supply voltage, nominal program and erase time

2. Typically, 3 lots, 77 units per lot

3. Generally, the typical endurance evaluation is performed on a single product of the family.

Typical Endurance for Motorola NVM Technologies

Using the above definition, the following NVM technologies from Motorola are capable of achieving significant margin to the minimum specified number of W/E cycles.

Table 1. Typical Endurance for Motorola NVM Technologies

Technology	Specification		Typical Number of Cycles at 25°C
	Number of Cycles	Temperature (°C)	
CDR1	100	–40 to 125	Not Characterized
CDR3	1 k	–40 to 125	>100 k
0.5µm SGF FLASH	10 k	–40 to 125	>100 k
0.5µm SGF EEPROM	10 k	–40 to 125	>100 k ⁽¹⁾
0.25µm SGF FLASH	10 k	–40 to 125	>100 k ⁽²⁾
0.25µm SGF EEPROM	10 k	–40 to 0	>300 k ⁽²⁾
	100 k	0 to 125	

1. EEPROM typical endurance value is based on the FLASH characterization

2. The following HCS12 devices use an earlier generation of the FLASH and are not covered by this engineering bulletin: MC9S12DT256B, MC9S12DJ256B, MC9S12A256B, MC9S12DG128B, MC9S12DJ128B, MC9S12DT128B, MC9S12A128B. These devices have, or will be, upgraded to current FLASH technology that is covered here and then will be available as MC9S12DT256, MC9S12DJ256, MC9S12A256, MC9S12DG128, MC9S12DJ128, MC9S12DT128, and MC9S12A128. Other devices using the earlier generation of the FLASH and not covered by this engineering bulletin are: MMC2114CFCVF33, MMC2114CFCPU33, MMC2114CFCPU33, MMC2113CFCVF33, MMC2113CFCPU33, MMC2113CFCPU33; DSP56F801, DSP56F802, DSP56F803, DSP56F805, DSP56F807, DSP56F826, and DSP56F827.



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