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Typical Data Retention for Nonvolatile Memory

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Introduction

This document explains how Freescale Semiconductor defines typical data retention in the product specification of nonvolatile memory (NVM).

Definition

Data retention refers to the ability of a memory bit to retain its data state over long periods of time regardless of whether the part is powered on or powered off.

Freescale Semiconductor guarantees a minimum data retention life in its product specification (generally 10 to 20 years). In practice, our technologies are capable of producing much longer lifetimes than the specified minimum. To give a better representation of the data retention life that can be achieved for most parts under nominal conditions, Freescale Semiconductor also provides a typical value in the product specification.

Freescale Semiconductor defines typical data retention by de-rating the intrinsic data retention capability of a technology to a normalized use condition.

This product incorporates SuperFlash® technology licensed from SST.

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Definition

The intrinsic data retention is by definition inherent to all bits manufactured with the same process technology. It is an estimate, based on accelerated stress data and the Arrhenius model, of the data retention life that most bits are expected to achieve.

The Arrhenius model is an industry standard for estimating data retention life of floating gate technologies. It is used to find the acceleration factor between a stress temperature and a use condition, which in turn can be used to de-rate results from an accelerated stress test.

The temperature acceleration factor is defined as:

$AF = \exp[(Ea/k) * (1/T_{Use} - 1/T_{Stress})]$

*Where*Ea is the intrinsic activation energy (eV)

k is Boltzmanns' constant (8.617×10^{-5} eV/K)(K = –273.16°C)

T_{Use} = use temperature (K)

T_{Stress} = stress temperature (K)

During the technology certification process, Freescale Semiconductor determines the intrinsic activation energy Ea for a technology with empirical data. This is done by evaluating time-to-failure under high temperature stress.

Typical data retention at a nominal use condition is calculated using the Arrhenius model with the measured activation energy and accelerated stress data from one of the following:

- Technology certification[1]
- Product qualification[2]
- Wafer bake[3]

Example

With a default activation energy of 0.8 eV[4],

- 1008 hours at 150°C (qualification bake time) is equivalent to 1150 years at 25°C
- 24 hours at 250°C (wafer bake time) is equivalent to 1800 years at 25°C
- 1008 hours at 150°C (qualification bake time) is equivalent to 60 years at 55°C
- 24 hours at 250°C (wafer bake time) is equivalent to 100 years at 55°C

1. Typically, extended bake on large sample at 150°C
2. Typically, 1008 hours at 150°C
3. Typically 250°C
4. Ea = 0.8 eV is a conservative estimate for the intrinsic activation energy supported by years of NVM experience. Freescale Semiconductor uses this value as the default activation energy for intrinsic data retention when empirical data are not available.

Typical Data Retention for Freescale Semiconductor NVM Technologies

Using the above definition, the following NVM technologies from Freescale Semiconductor are capable of achieving greater than 100 years of intrinsic data retention.

Table 1. Typical Data Retention Time Based on the Qualification Bake Time and the Activation Energy of Each Technology

Technology	Ea (eV)	Minimum Specification		Qualification Stress		Typical Data Retention (Yr) @ 25°C
		Time (Yr)	Temp (°C)	Time (Hr)	Temp (°C)	
CDR1	0.92(1)	10	85	1008	150	>100
CDR3	1.2(1)	10/15	125/85	1008	150	>100
0.5µm SGF	0.8(2)	15	125	504	175	>100
0.25µm SGF	0.8(2)	15	85(3)	1008	150	>100(4)

NOTES:
1. Measured by Freescale Semiconductor
2. Default value
3. Average junction temperature
4. The following HCS12 devices use an earlier generation of the FLASH and are not covered by this engineering bulletin: MC9S12DT256B, MC9S12DJ256B, MC9S12A256B, MC9S12DG128B, MC9S12DJ128B, MC9S12DT128B, MC9S12A128B. These devices have, or will be, upgraded to current FLASH technology that is covered here and then will be available as MC9S12DT256, MC9S12DJ256, MC9S12A256, MC9S12DG128, MC9S12DJ128, MC9S12DT128, and MC9S12A128. Other devices using the earlier generation of the FLASH and not covered by this engineering bulletin are: MMC2114CFCVF33, MMC2114CFCPV33, MMC2114CFCPU33, MMC2113CFCVF33, MMC2113CFCPV33, MMC2113CFCPU33; DSP56F801, DSP56F802, DSP56F803, DSP56F805, DSP56F807, DSP56F826, and DSP56F827.

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