# TEA18363T/2

## GreenChip SMPS control IC

Rev. 1 — 6 March 2023 Product data sheet

## 1 General description

The TEA18363T is a controller IC for low-cost switched-mode power supplies (SMPS). It is intended for flyback topologies. The built-in green functions provide high efficiency at all power levels.

At high power levels, the flyback operates in quasi-resonant (QR) mode. At lower power levels, the controller switches to frequency reduction (FR) or discontinuous conduction mode (DCM) and limits the peak current to approximately 25 % of the maximum peak current. Valley switching is used in all operating modes.

At low power levels, when the flyback switching frequency drops below 25 kHz, the flyback converter switches to burst mode. A special burst mode has been integrated which reduces the optocurrent to a minimum level, ensuring high efficiency at low power and excellent no-load power performance. As the switching frequency in this mode has a minimum value of 25 kHz while the burst frequency is below 800 Hz, the frequencies are outside the audible range. During the non-switching phase of the burst mode, the internal IC supply current is minimized for further efficiency optimization.

The TEA18363T includes an accurate overpower protection (OPP). The OPP enables the controller to operate in overpower situations for a limited time. If the output is shorted, the system switches to low-power mode where the output power is limited to a lower level.

The TEA18363T is manufactured in a high-voltage silicon-on-insulator (SOI) process. The SOI process combines the advantages of a low-voltage process (accuracy, high-speed protection, functions, and control), while maintaining the high-voltage capabilities (high-voltage start-up, low standby power, and an integrated X-capacitor discharge function).

The TEA18363T enables low-cost, highly efficient, and reliable supplies for power requirements up to 75 W to be designed with a minimum number of external components.

All values mentioned in this data sheet are typical values, unless otherwise specified.

# 2 Features and benefits

## 2.1 General features

- SMPS controller IC for low-cost applications
- Large supply voltage range (up to 30 V)
- Integrated high-voltage start-up
- Continuous VCC regulation during start-up and protection via the HV pin, allowing a minimum VCC capacitor value
- Reduced optocurrent in burst mode enabling low no load power consumption
- Operating frequencies in all operating modes are outside the audible area
- Integrated X-capacitor discharge; NXP Semiconductors patented (Patent reference: 81512184EP01)
- Adjustable soft start

## 2.2 Green features

- Low supply current during normal operation (0.6 mA without load)
- Low supply current during non-switching state in burst mode (0.2 mA)
- Valley switching for minimum switching losses
- Frequency reduction with fixed minimum peak current to maintain high efficiency at low output power levels

## 2.3 Protection features

- Mains voltage independent overpower protection (OPP)
- Overtemperature protection (OTP)
- Integrated overpower timeout
- Integrated restart timer for system fault conditions
- Continuous mode protection using demagnetization detection
- Accurate overvoltage protection (OVP)
- Driver maximum on-time protection

# 3 Applications

- Applications requiring efficient and cost-effective power supply solutions up to 75 W

# 4 Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| TEA18363T/2 | SO8 | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |

# 5 Marking

**Table 2. Marking**

| Type number | Marking code |
|---|---|
| TEA18363T/2 | EA18363 |

# 6 Block diagram

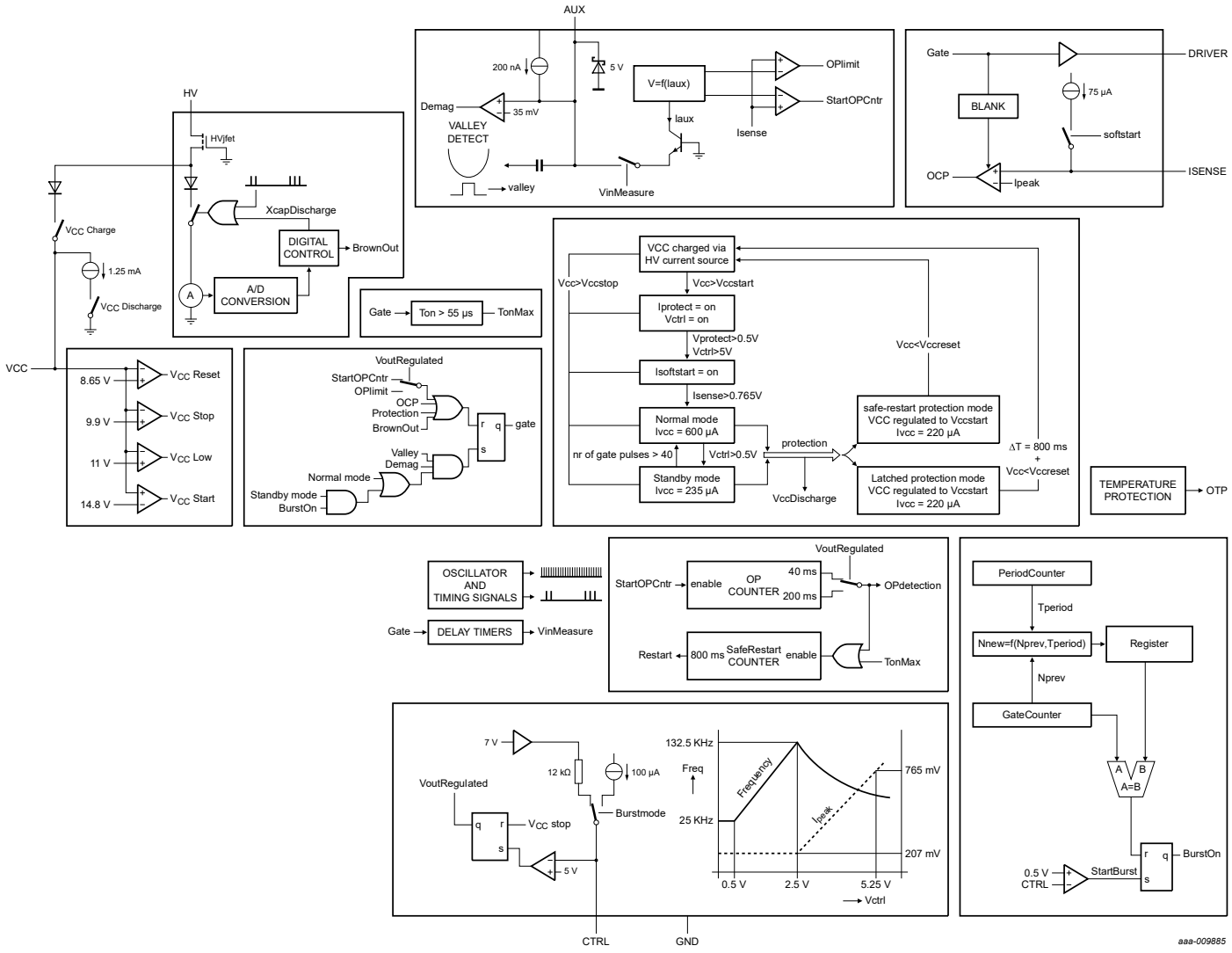



**Figure 1. Block diagram**

# 7 Pinning information

## 7.1 Pinning

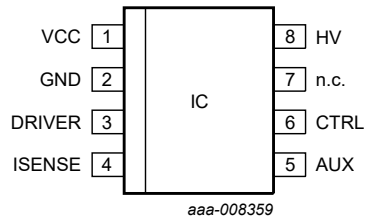



**Figure 2. TEA18363T pinning diagram (SOT96-1)**

## 7.2 Pin description

**Table 3. Pin description**

| Pin | Pin number | Description |
|---|---|---|
| VCC | 1 | supply voltage |
| GND | 2 | ground |
| DRIVER | 3 | gate driver output |
| ISENSE | 4 | current sense input |
| AUX | 5 | auxiliary winding input for demagnetization timing, valley detect, overpower correction, and OVP |
| CTRL | 6 | control input |
| n.c. | 7 | not connected |
| HV | 8 | high-voltage start-up; active X-capacitor discharge |

# 8 Functional description

## 8.1 General control

Figure 3 shows a typical configuration of the TEA18363T, including flyback circuit controller.

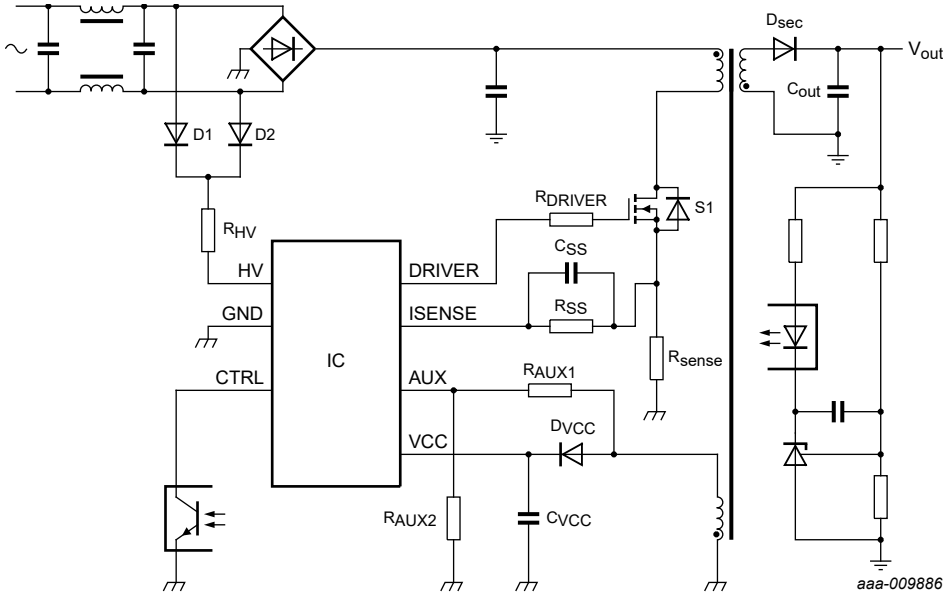



**Figure 3. Typical TEA18363T configuration**

### 8.1.1 Start-up and undervoltage lockout (UVLO)

Initially, the capacitor on the VCC pin is charged from the high-voltage mains using the HV pin. As long as $V_{CC}$ is below $V_{startup}$, the IC current consumption is minimized to 40 µA.

When $V_{CC}$ reaches the $V_{startup}$ level, the control logic activates the internal circuitry. The IC then waits for the CTRL pin to reach $V_{startup(CTRL)}$, and the mains voltage to increase to above the brownin level. When both conditions are met, the soft start capacitor on the ISENSE pin ($C_{SS}$ in Figure 3) is charged. The system starts switching. In a typical application, the auxiliary winding of the transformer takes over the supply voltage.

During the start-up period, the VCC pin is continuously regulated to the $V_{startup}$ level. To achieve the continuous regulation, the HV charge current is used until the output voltage is at its regulation level, which is detected via the CTRL pin. In this way, the VCC capacitor value can be limited. Due to the limited current capability from the HV pin and depending on the mains voltage, the voltage on pin VCC can still drop slightly during the start-up period.

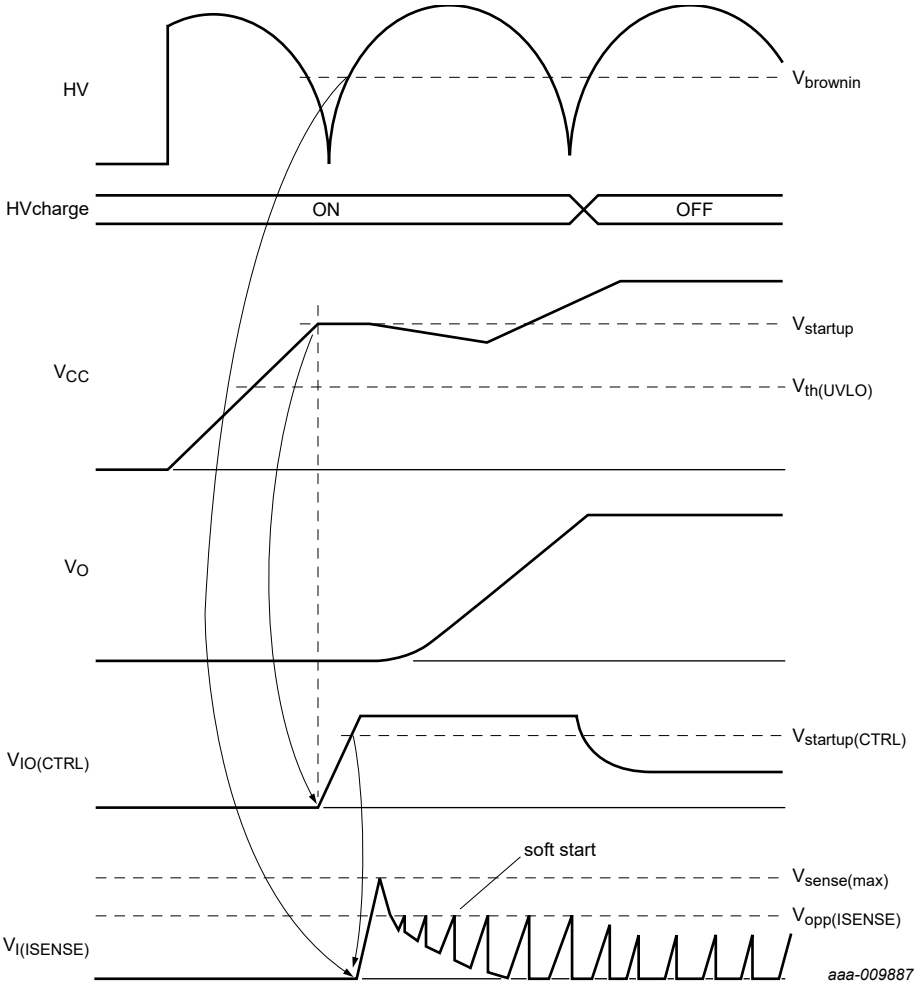



**Figure 4. Start-up sequence and normal operation**

## 8.2 Modes of operation

The TEA18363T operates in quasi-resonant mode, discontinuous conduction mode, or burst mode (see Figure 5). The auxiliary winding of the flyback transformer provides demagnetization and valley detection.

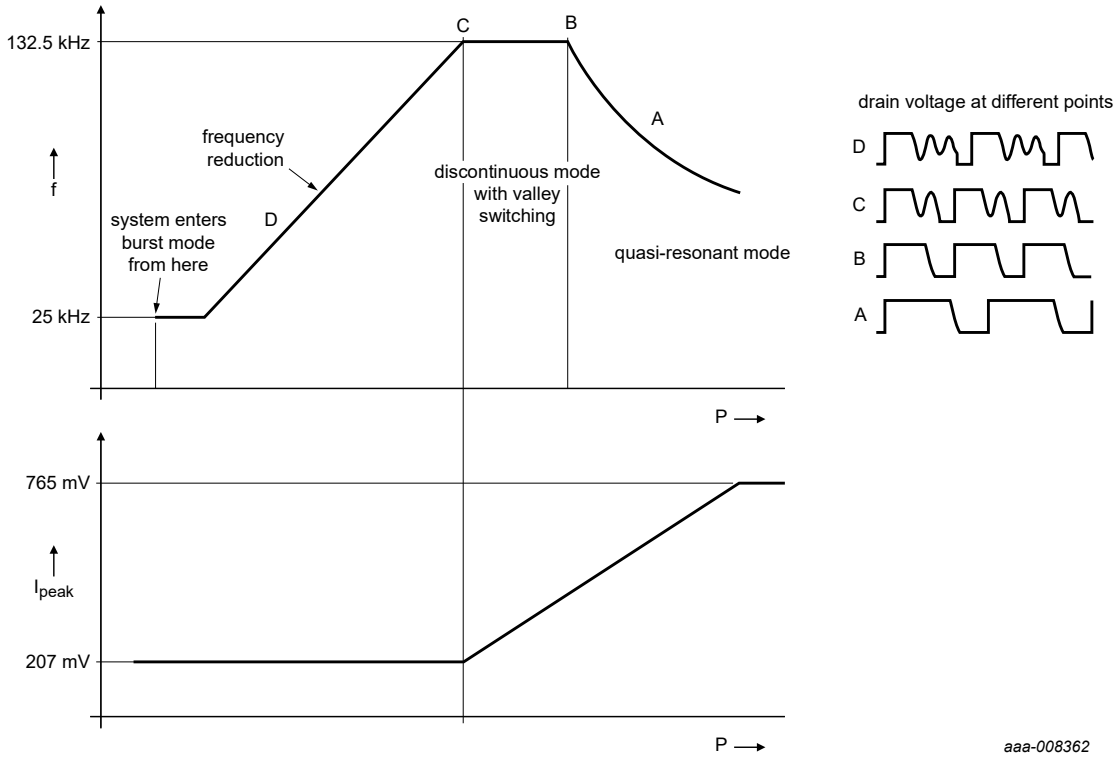



**Figure 5. Operation modes**

At high output power, the converter operates in quasi-resonant mode. The next converter cycle starts after demagnetization of the transformer and detection of the valley. In quasi-resonant mode, switching losses are minimized because the external MOSFET is switched on while the drain-source voltage is minimal.

To prevent high-frequency operation at lower loads, the quasi-resonant operation switches to discontinuous conduction mode (DCM) operation with valley skipping once the frequency reaches its maximum. This frequency limit reduces the MOSFET switch-on losses and conducted EMI.

At medium power levels, the controller enters frequency reduction (FR) mode. A voltage controlled oscillator (VCO) controls the frequency. The minimum frequency in this mode is reduced to 25 kHz. During FR mode, the primary peak current is kept at an adjustable minimum level to maintain high efficiency. Valley switching is also active in this mode.

At low power, the converter enters the burst mode. In burst mode, the minimum switching frequency is 25 kHz.

## 8.3 Supply management

All internal reference voltages are derived from a temperature-compensated on-chip band gap circuit. Internal reference currents are derived from a trimmed and temperature-compensated current reference circuit.

## 8.4 Mains voltage measuring

In a typical application, the mains input voltage is measured using the HV pin. Once per ms, the mains voltage is measured by pulling down the HV pin to ground and measuring its current. This current then reflects the input voltage.

The system determines if the mains voltage exceeds the brownin level or it is disconnected using an analog-to-digital converter and digital control (see Figure 1).

When the mains exceeds the brownin level, the system is allowed to start switching (see Figure 6).

If the mains voltage is continuously below the brownout level for at least 30 ms, a brownout is detected and the system immediately stops switching. This period is required to avoid that the system stops switching due to the zero crossings of the mains or during a short mains interruption.

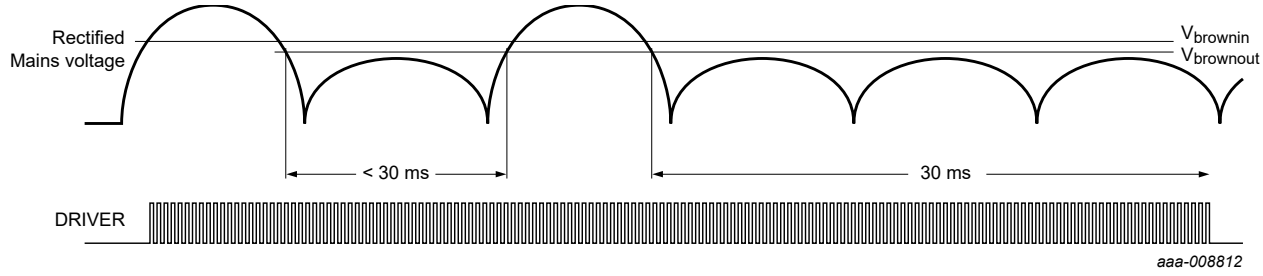



**Figure 6. Mains voltage measuring**

When the mains voltage is measured by pulling the HV pin to ground, the digital control calculates if there is a positive dV/dt at the mains. A positive dV/dt implies that a mains is connected.

When a mains is detected, the measuring of the mains input voltage is stopped for 6 ms to improve efficiency. To improve efficiency, this waiting period is extended to 97 ms in burst mode.

When succeeding samples cross the brownin level ($I_{bi(HV)}$) or the mains high level ($I_{IH(HV)}$; see Figure 7), a positive dV/dt is measured.

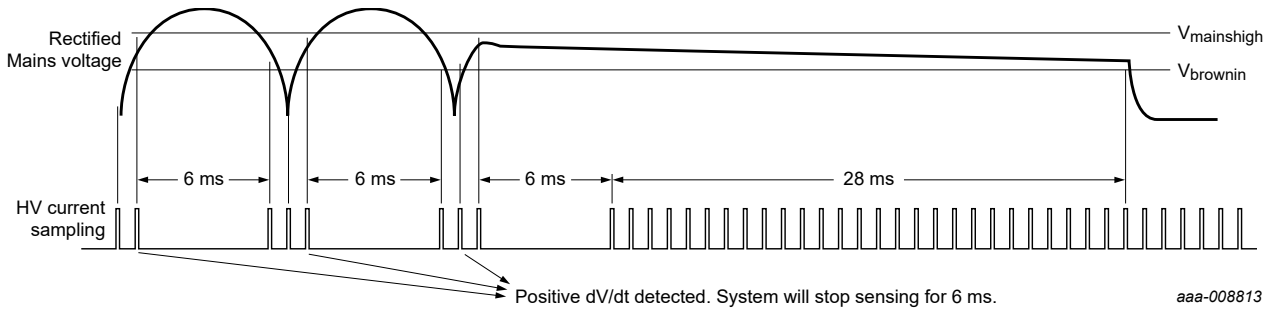



**Figure 7. Detecting mains connection by +dV/dt**

If the system does not detect a positive dV/dt for 28 ms, it assumes that the mains is disconnected. In that case, the HV pin is continuously pulled to ground, discharging the external X-capacitor.

## 8.5 Auxiliary winding

The VCC pin is connected via a diode and a capacitor to the auxiliary winding to supply the control IC efficiently.

To detect demagnetization, valley, and input and output voltage, the auxiliary winding is connected to the AUX pin via a resistive divider (see Figure 3). Each switching cycle is divided in sections. During each section, the system knows if the voltage or current out of the AUX pin reflects the demagnetization, valley, or input/output voltage (see Figure 8).

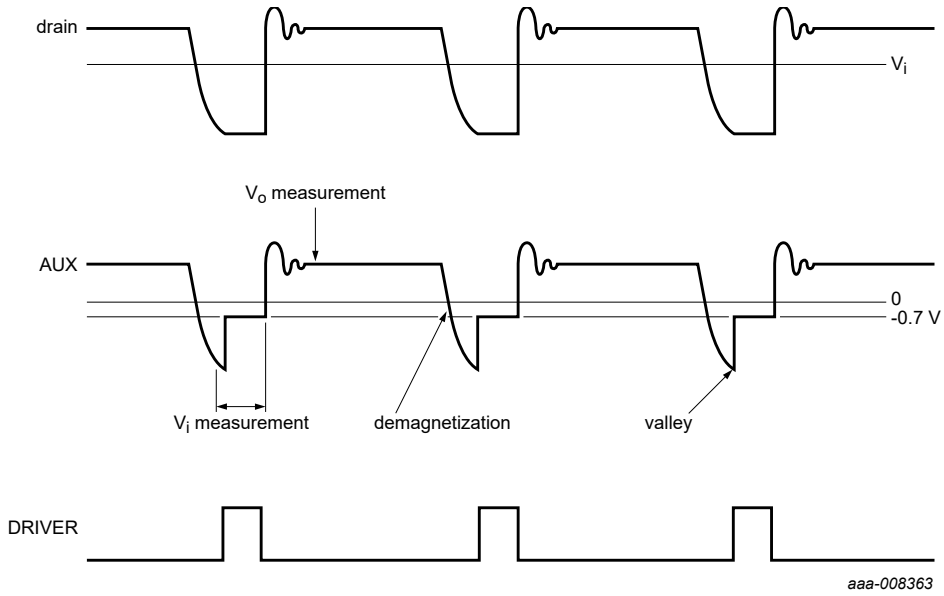



**Figure 8. AUX pin used for demagnetization, valley, and input and output voltage measurement**

When the external MOSFET is switched on, the voltage at the auxiliary winding reflects the input voltage. The AUX pin is clamped to −0.7 V. The output current is a measure of the input voltage. This current value is internally used for an accurate OPP.

The demagnetization, valley, and output voltages are measured as a voltage on the AUX pin. In this way, the input voltage measurement and OVP can be adjusted independently.

## 8.6 Protections

If a protection is triggered, the controller stops switching. Depending on the protection triggered and the IC version, the protection causes a restart or latches the converter to an off state (see Table 4).

To avoid false triggering, some protections have a built-in delay.

**Table 4. Protections overview**

| Protection | Delay | Action | $V_{CC}$ regulated |
|---|---|---|---|
| AUX open | no | wait until AUX is connected | no |
| brownout | 30 ms | wait until $V_{mains} > V_{brownin}$ | yes |
| maximum on-time | no | safe restart 800 ms | yes |

**Table 4. Protections overview**...*continued*

| Protection | Delay | Action | $V_{CC}$ regulated |
|---|---|---|---|
| OTP internal | no | latch | yes |
| OVP via the AUX pin | 4 driver pulses | latch | yes |
| overpower compensation | no | via AUX; cycle-by-cycle | - |
| overpower timeout | 40 ms or 200 ms | safe restart 800 ms | yes |
| overpower and UVLO | no | safe restart 800 ms | yes |
| overcurrent protection | blanking time | cycle-by-cycle | no |
| UVLO | no | Wait until $V_{CC} > V_{startup}$ | yes |

When the system stops switching, the VCC pin is not supplied via the auxiliary winding anymore. Depending on the protection triggered, the VCC is regulated to $V_{startup}$ via the HV pin (see Table 4).

Releasing the latched protections or shortening the safe restart timer can be achieved by removing or shorting the mains voltage. It is called a fast latch reset. It is used to shorten the test time in production (See Section 8.7).

### 8.6.1 Overpower protection (OPP)

The overpower function is used to realize a maximum output power which is nearly constant over the full input mains.

The overpower compensation circuit measures the input voltage via the AUX pin and outputs two reference voltages (see Figure 1). If the measured voltage at the ISENSE pin exceeds the highest reference voltage ($V_{opc(ISENSE)}$), the DRIVER output is pulled low. If the measured ISENSE voltage exceeds the lower reference voltage ($V_{opp(ISENSE)}$), the overpower counter starts. Both reference voltages depend on the measured input voltage. In this way, the system allows 150 % overpower over the rated power on a cycle-by-cycle base. 100 % overpower triggers the overpower counter of 200 ms. Figure 9 shows the overpower protection curves.

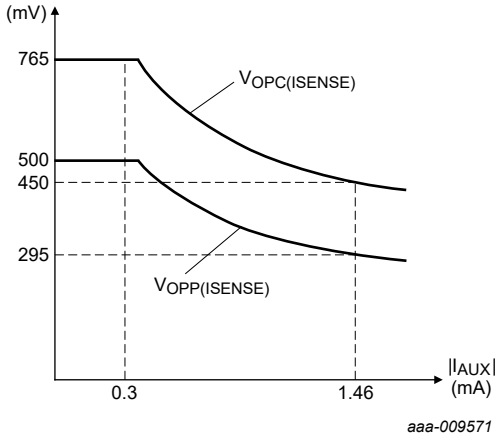



**Figure 9. Overpower protection curves**

During system start-up, the maximum overpower is limited to 100 % and the maximum timeout period is lowered to 40 ms. When the output voltage is within its regulation level (voltage on the CTRL pin is below 5 V), the maximum overpower is switched to 150 %. The maximum timeout period returns to 200 ms, which limits the output power to a minimum at a shorted output. Lowering the maximum output power and shortening the overpower timer ensure that the input power of the system is limited to < 5 W at a shorted output.

Due to the limited output power, the output voltage drops if the load requires more than 150 %. As a result, the $V_{CC}$ voltage drops as well and UVLO can be triggered. To retain the same response in an overpower situation (whether UVLO is triggered or not) the system enters the protection mode (latch or safe restart) when overpower and UVLO is detected. The system entering the protection mode does not depend on the value of the OP counter.

### 8.6.2 Overvoltage protection (OVP)

An accurate output OVP is implemented by measuring the voltage at the AUX pin during the secondary stroke. As the auxiliary winding voltage is a well-defined replica of the output voltage, the external resistor divider ratio $R_{AUX2}$ / ($R_{AUX1}$ + $R_{AUX2}$) can adjust the OVP level.

An internal counter of four gate pulses prevents false OVP detection which can occur during ESD or lightning events.

### 8.6.3 Overtemperature protection (OTP)

If the junction temperature exceeds the thermal temperature shutdown limit, integrated OTP ensures that the IC stops switching. OTP is a latched protection.

### 8.6.4 Maximum on-time

The controller limits the on-time of the external MOSFET to 55 µs. When the on-time is longer, the IC stops switching and enters safe restart mode.

### 8.6.5 Safe restart

If a protection is triggered and the system enters the safe restart mode, the system restarts after 800 ms. Because the system is not switching, the VCC pin is supplied from the mains via the HV pin.

After the 800 ms, the control IC measures the mains voltage. If the mains voltage exceeds the brownin level, the control IC activates the internal voltage sources connected to the CTRL pin. When the voltage on the CTRL pin reaches a minimum level, the soft start capacitor on the ISENSE pin is charged and the system starts switching again.

The $V_{CC}$ is continuously regulated to the $V_{startup}$ level until the output voltage is within the regulation level again.

### 8.6.6 Latched protection

If a protection is triggered and the system enters the latched protection mode, the $V_{CC}$ is continuously regulated to the $V_{startup}$ level via the HV current source. As long as the AC voltage remains, the system does not switch.

Removing the mains for a short time is the only possibility to restart the system.

### 8.6.7 Fast latch reset

Fast latch reset is a simple and fast method to reset the system when it is in latched protection mode or safe restart mode. This function is used during production testing.

When the latched protection mode or safe restart mode is triggered, an internal current source ($I_{CC(dch)}$) fast discharges the voltage on pin VCC (see Figure 10). If the VCC voltage is high, the fast discharge avoids an additional waiting period. When shorting the mains, the waiting period is only the time of the discharge from $V_{startup}$ to $V_{rst}$.

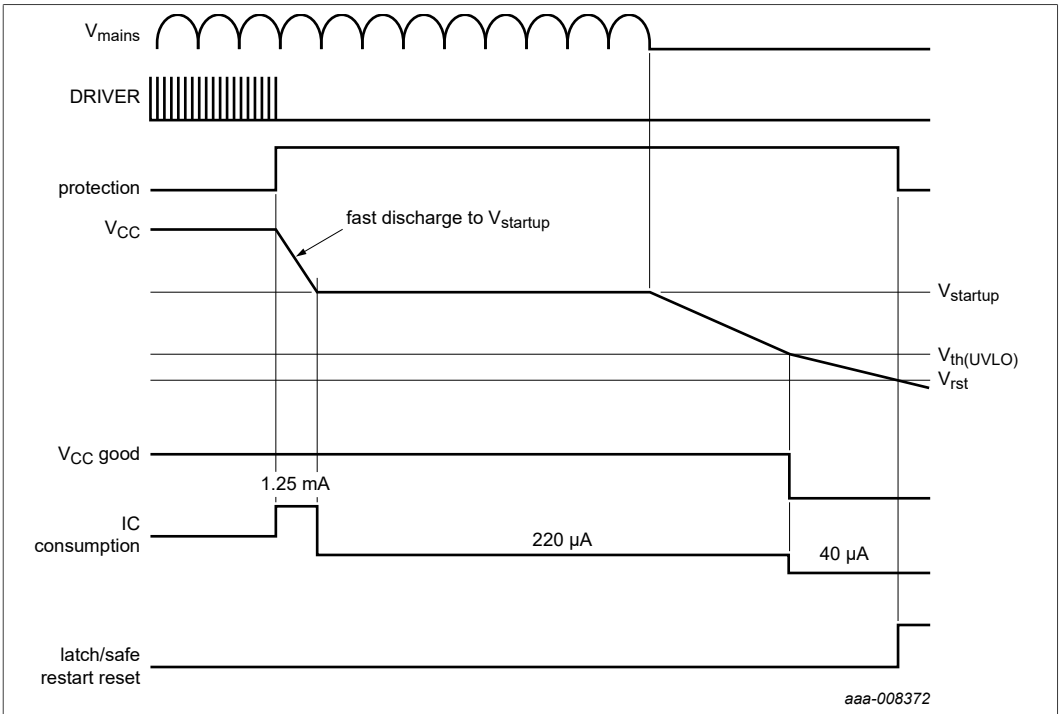



**Figure 10. Fast latch reset**

Using a 10 µF VCC capacitor, the fast latch reset time is < 0.6 s. If the mains is not shorted but removed, a discharge of the X-capacitor can cause an additional waiting time.

## 8.7 Burst mode operation (CTRL pin)

The controller enters the burst mode when a low output power causes the voltage on the CTRL pin to drop below 0.5 V.

During normal operation, the primary optocurrent can be calculated with Equation 1:

$$I_{opto} = \frac{\left(7\ V - V_{IO(CTRL)}\right)}{12\ k\Omega} \quad (1)$$

So, without any additional measure, the maximum primary optocurrent in burst mode is:

$$I_{opto} = \frac{(7\ V - 0\ V)}{12\ k\Omega} = 583\ \mu A$$

Depending on the optocoupler used, the secondary optocurrent is even higher.

To achieve minimum no-load input power, the internal voltage (7 V) is regulated to a value that causes the primary optocurrent value to be 100 µA when the system is in burst mode. The secondary optocurrent is then automatically also within this lower range. If the IC detects that the optocurrent is lower than 80 µA, the internal voltage is increased faster to achieve a small output voltage undershoot at a positive load step. Once the system enters normal operation mode, the internal voltage is slowly increased to 7 V again.

To avoid audible noise, a special digital burst mode is implemented. The minimum switching frequency in this mode is 25 kHz. The burst mode repetition rate has a target frequency of 800 Hz (1250 µs; see Figure 11).

The requested output power defines the number of pulses at each burst period. At higher output power, the number of switching pulses increases. At low load, it decreases.

The digital circuit defines the number of burst cycles so that the burst frequency is below the audible range (800 Hz) and the switching frequency exceeds the audible range (25 kHz). Any audible noise is avoided.

The minimum number of switching cycles is set to 3 to ensure good efficiency at very low loads. To regulate the output power at a very low load, the system increases the burst period (< 800 Hz). The increased burst period is still outside the audible range.

To improve the no-load input power and efficiency at low loads further, the current consumption of the IC is lowered to 235 µA during the non-switching period in the burst mode.

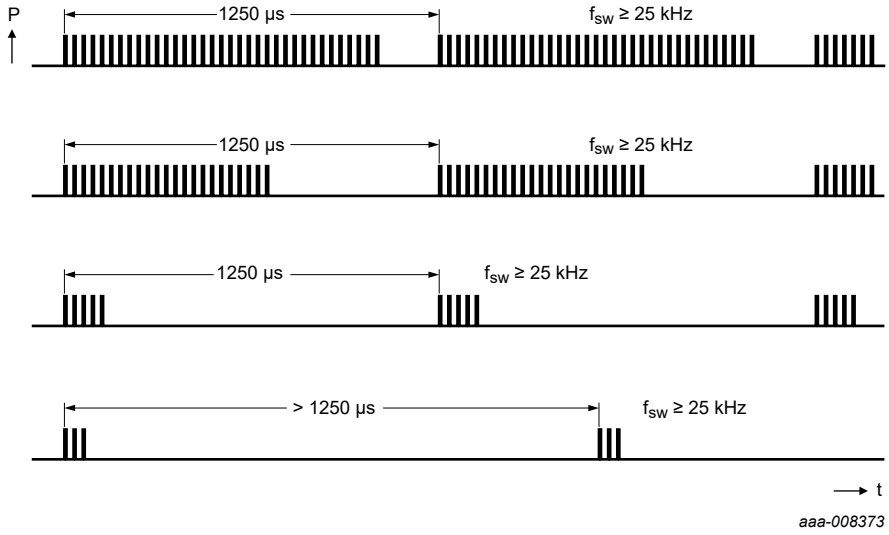



**Figure 11. Burst mode operation**

To achieve a good transient response in burst mode, the system starts switching immediately at an increased output load, allowing a shorter burst period. Eventually, it regulates to the required burst period by increasing the number of driver pulses (see Figure 12).

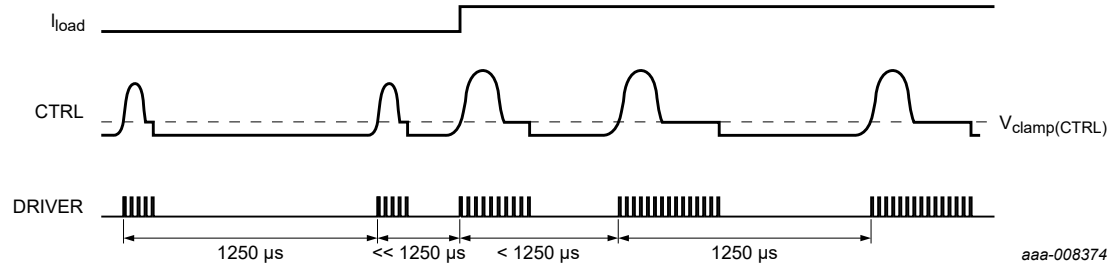
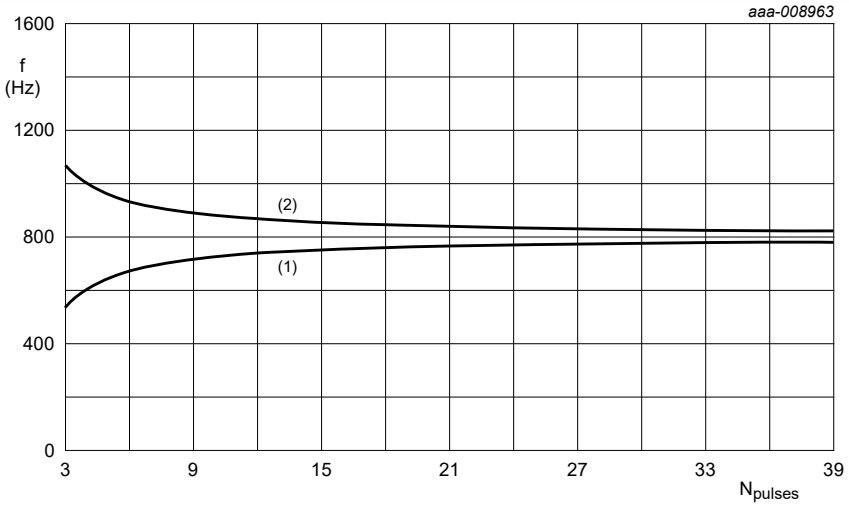



**Figure 12. Transient response in burst mode**

Due to the discrete number of switching cycles, the new calculated number of pulses must be 0.5 higher or lower than the existing number before one switching cycle is added or taken away. For the IC to increase or decrease the number of switching cycles, a certain deviation from the target burst repetition frequency (800 Hz) is required because of the internal algorithm. This deviation becomes smaller when the number of switching cycles increases. Figure 13 shows the upper and lower limits of the burst repetition frequency as a function of the number of pulses.




(1) Lower limit
(2) Upper limit

**Figure 13. Upper and lower limits of burst frequency**

When the number of driver pulses within one burst period exceeds 40, the system switches to normal mode again.

During the burst period, the voltage on the CTRL pin is clamped to the minimum $V_{clamp(CTRL)}$. The current out of the CTRL pin is measured. If the current exceeds $I_{stop(CTRL)}$, the burst period is terminated regardless of digital control. This feature ensures a small overshoot at the output voltage when the load in burst mode suddenly reduces. At the end of each burst period, the CTRL pin is pulled to the ground level for 12.5 µs, unless the current flowing from pin CTRL < 87 µA. This value usually occurs at a positive load step.

## 8.8 Soft start-up (ISENSE pin)

To prevent audible noise during start-up or a restart condition, a soft start feature is implemented. Before the converter starts, the soft start capacitor $C_{SS}$ on the ISENSE pin is charged. When the converter starts switching, the primary peak current slowly increases as the soft start capacitor discharges through the soft start resistor $R_{SS}$ (see Figure 3).

The external soft start capacitor and the parallel resistor values set the soft start time constant.

## 8.9 Driver (DRIVER pin)

The driver circuit to the gate of the power MOSFET has a current sourcing capability of 300 mA and a current sink capability of 750 mA. These capabilities allow a fast turn-on and turn-off of the power MOSFET for efficient operation.

The maximum driver output is limited to 10.5 V. The DRIVER output pin can be connected to the gate of a MOSFET directly or via a resistor.

# 9 Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| **Voltages** | | | | | |
| $V_{IO(HV)}$ | input/output voltage on pin HV | | −0.4 | +700 | V |
| $V_{CC}$ | supply voltage | continuous | −0.4 | +30 | V |
| | | t < 100 ms | - | +35 | V |
| $V_{IO(CTRL)}$ | input/output voltage on pin CTRL | | −0.4 | +12 | V |
| $V_{I(ISENSE)}$ | input voltage on pin ISENSE | | −0.4 | +12 | V |
| $V_{IO(AUX)}$ | input/output voltage on pin AUX | current limited | −5 | +5 | V |
| $V_{O(DRIVER)}$ | output voltage on pin DRIVER | | −0.4 | +12 | V |
| **Currents** | | | | | |
| $I_{IO(AUX)}$ | input/output current on pin AUX | | −1.5 | +1 | mA |
| $I_{IO(HV)}$ | input/output current on pin HV | | −1 | +5 | mA |
| $I_{IO(CTRL)}$ | input/output current on pin CTRL | | −3 | 0 | mA |
| $I_{O(DRIVER)}$ | output current on pin DRIVER | δ < 10 % | −0.4 | +1 | A |
| **General** | | | | | |
| $P_{tot}$ | total power dissipation | $T_{amb}$ < 75 °C | - | 0.82 | W |
| $T_{stg}$ | storage temperature | | −55 | +150 | °C |
| $T_j$ | junction temperature | | −40 | +150 | °C |
| **Electrostatic discharge (ESD)** | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | class 1 | | | |
| | | human body model (HBM)[1] | | | |
| | | pin HV | −1000 | +1000 | V |
| | | all other pins | −2000 | +2000 | V |
| | | charged device model (CDM)[2] | −500 | +500 | V |

[1] Equivalent to discharge a 100 pF capacitor through a 1.5 kΩ series resistor.
[2] Equivalent to discharge a 200 pF capacitor through a 0.75 µH coil and 10 Ω.

## 10 Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air; JEDEC test board | 91 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | in free air; JEDEC test board | 37.8 | K/W |

# 11 Characteristics

**Table 7. Characteristics**

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Start-up current source (HV pin)** | | | | | | |
| $I_{startup(HV)}$ | start-up current on pin HV | $V_{HV}$ > 10 V | 0.8 | 1.1 | 1.4 | mA |
| | | $V_{CC}$ > $V_{startup}$; HV not sampling | - | - | 1 | µA |
| $V_{clamp}$ | clamp voltage | $I_{HV}$ < 2 mA | - | - | 680 | V |
| **Supply voltage management (VCC pin)** | | | | | | |
| $V_{startup}$ | start-up voltage | | 13.4 | 14.9 | 16.4 | V |
| $V_{restart}$ | restart voltage | burst mode | 9.9 | 11 | 12.1 | V |
| $V_{th(UVLO)}$ | undervoltage lockout threshold voltage | | 9 | 9.9 | 10.8 | V |
| $V_{rst}$ | reset voltage | | 7.75 | 8.65 | 9.55 | V |
| $I_{CC(startup)}$ | start-up supply current | $V_{HV}$ = 0 V | - | 40 | - | µA |
| | | $V_{HV}$ > 10 V | −1.35 | −1.05 | −0.75 | mA |
| $I_{CC(oper)}$ | operating supply current | driver unloaded; excluding optocurrent | 500 | 600 | 700 | µA |
| $I_{CC(burst)}$ | burst mode supply current | non-switching; excluding optocurrent | 200 | 235 | 270 | µA |
| $I_{CC(prot)}$ | protection supply current | | 185 | 220 | 255 | µA |
| $I_{CC(dch)}$ | discharge supply current | latched protection; $V_{CC}$ > $V_{startup}$ | 0.9 | 1.25 | 1.6 | mA |
| **Mains detect (HV pin)** | | | | | | |
| $t_{p(HV)}$ | pulse duration on pin HV | measuring mains voltage | 18 | 20 | 22 | µs |
| $f_{meas(HV)}$ | measurement frequency on pin HV | measuring mains voltage | 0.9 | 1.0 | 1.1 | kHz |
| $t_{d(norm)HV}$ | normal mode delay time on pin HV | measuring mains voltage | 5 | 6 | 7 | ms |
| $t_{d(burst)HV}$ | burst mode delay time on pin HV | measuring mains voltage | 87 | 97 | 107 | ms |
| $I_{bo(HV)}$ | brownout current on pin HV | | 552 | 587 | 622 | µA |
| $I_{bi(HV)}$ | brownin current on pin HV | | 623 | 663 | 703 | µA |
| $I_{bo(hys)HV}$ | hysteresis of brownout current on pin HV | | - | 76 | - | µA |
| $I_{IH(HV)}$ | HIGH-level input current on pin HV | | 1186 | 1262 | 1338 | µA |
| $I_{IL(HV)}$ | LOW-level input current on pin HV | | 1118 | 1190 | 1262 | µA |
| $I_{HL(hys)HV}$ | HIGH to LOW hysteresis current on pin HV | | - | 72 | - | µA |
| $I_{clamp(HV)}$) | clamp current on pin HV | during measurement time | - | - | 1.7 | mA |
| $V_{meas(HV)}$ | measurement voltage on pin HV | brownin/brownout | - | 2.6 | - | V |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{d(dch)}$ | discharge delay time | X capacitor discharge; pin HV | - | 28 | - | ms |
| $t_{d(det)bo}$ | brownout detection delay time | | - | 30 | - | ms |
| **Peak current control (pin CTRL)** | | | | | | |
| $V_{IO(CTRL)}$ | input/output voltage on pin CTRL | minimum flyback peak current | 2.3 | 2.5 | 2.7 | V |
| | | maximum flyback current | 4.9 | 5.25 | 5.6 | V |
| $R_{int(CTRL)}$ | internal resistance on pin CTRL | | 10 | 12 | 14 | kΩ |
| $I_{IO(CTRL)}$ | input/output current on pin CTRL | normal mode | | | | |
| | | $V_{CTRL}$ = 1.5 V | −0.58 | −0.48 | −0.38 | mA |
| | | $V_{CTRL}$ = 3.5 V | −0.385 | −0.315 | −0.245 | mA |
| $V_{startup(CTRL)}$ | start-up voltage on pin CTRL | | 4.7 | 5 | 5.3 | V |
| **Burst mode (pin CTRL)** | | | | | | |
| $V_{th(burst)}$ | burst mode threshold voltage | | 0.42 | 0.5 | 0.58 | V |
| $T_{burst}$ | burst mode period | | - | 1250 | - | µs |
| $f_{sw(min)}$ | minimum switching frequency | burst mode | 23 | 25 | 27 | kHz |
| $I_{REGD(CTRL)}$ | regulated current on pin CTRL | burst mode | −115 | −100 | −85 | µA |
| $V_{clamp(CTRL)}$ | clamp voltage on pin CTRL | burst mode; system switching | 0.44 | 0.5 | 0.56 | V |
| $I_{stop(CTRL)}$ | stop current on pin CTRL | burst mode; system switching; including regulated output current | −820 | −750 | −680 | µA |
| $t_{pd(CTRL)}$ | pull-down time on pin CTRL | | 10 | 12.5 | 15 | µs |
| $I_{det(CTRL)}$ | detection current on pin CTRL | positive load step | 65 | 80 | 95 | µA |
| | | disable pulling down the CTRL pin | 77 | 87 | 97 | µA |
| **Oscillator** | | | | | | |
| $f_{sw(max)}$ | maximum switching frequency | | 125 | 132.5 | 140 | kHz |
| $f_{sw(min)}$ | minimum switching frequency | | 23 | 25 | 27 | kHz |
| $V_{start(red)f}$ | frequency reduction start voltage | pin CTRL | 2.3 | 2.5 | 2.7 | V |
| **Current sense (pin ISENSE)** | | | | | | |
| $V_{sense(max)}$ | maximum sense voltage | ΔV/Δt = 0 V/s; $I_{AUX}$ = 0 µA; $V_{CTRL}$ = 5.5 V | 700 | 765 | 830 | mV |
| | | frequency reduction mode; ΔV/Δt = 0 mV/µs; $I_{AUX}$ = 0 µA; $V_{CTRL}$ = 1.0 V | 190 | 207 | 225 | mV |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PD(sense)}$ | sense propagation delay | from the ISENSE pin reaching $V_{sense(max)}$ to driver off; $V_{ISENSE}$ pulse-stepping 100 mV around $V_{sense(max)}$ | - | 120 | - | ns |
| $t_{leb}$ | leading edge blanking time | | 275 | 325 | 375 | ns |
| **Soft start (pin ISENSE)** | | | | | | |
| $I_{start(soft)}$ | soft start current | | −85 | −75 | −65 | µA |
| $V_{start(soft)}$ | soft start voltage | enable voltage | - | $V_{sense(max)}$ | | V |
| $R_{start(soft)}$ | soft start resistance | | 12 | - | - | kΩ |
| **Demagnetization and valley control (pin AUX)** | | | | | | |
| $V_{det(demag)}$ | demagnetization detection voltage | | 20 | 35 | 50 | mV |
| $I_{prot(AUX)}$ | protection current on pin AUX | | - | −200 | - | nA |
| $t_{blank(det)demag}$ | demagnetization detection blanking time | | 1.8 | 2.2 | 2.6 | µs |
| $(\Delta V/\Delta t)_{vrec}$ | valley recognition voltage change with time | positive ΔV/Δt | 0.25 | 0.37 | 0.49 | V/µs |
| | | negative ΔV/Δt | −2.35 | −1.9 | −1.45 | V/µs |
| $t_{d(vrec-swon)}$ | valley recognition to switch-on delay time | | - | 120 | - | ns |
| $V_{clamp(AUX)}$ | clamp voltage on pin AUX | $I_{AUX}$ = 1 mA | 4.4 | 4.8 | 5.2 | V |
| $t_{sup(xfmr\_ring)}$ | transformer ringing suppression time | | 1.9 | 2.3 | 2.7 | µs |
| **Maximum on-time (pin DRIVER)** | | | | | | |
| $t_{on(max)}$ | maximum on-time | | 45 | 55 | 65 | µs |
| **Driver (pin DRIVER)** | | | | | | |
| $I_{source(DRIVER)}$ | source current on pin DRIVER | $V_{DRIVER}$ = 2 V | - | −0.3 | −0.25 | A |
| $I_{sink(DRIVER)}$ | sink current on pin DRIVER | $V_{DRIVER}$ = 2 V | 0.25 | 0.3 | - | A |
| | | $V_{DRIVER}$ = 10 V | 0.6 | 0.75 | - | A |
| $V_{O(DRIVER)max}$ | maximum output voltage on pin DRIVER | | 9 | 10.5 | 12 | V |
| **Overpower compensation (pin ISENSE and pin AUX)** | | | | | | |
| $V_{clamp(AUX)}$ | clamp voltage on pin AUX | primary stroke; $I_{AUX}$ = −0.3 mA | −0.8 | −0.7 | −0.6 | V |
| $t_{d(clamp)AUX}$ | clamp delay time on pin AUX | after rising edge of pin DRIVER | 580 | 665 | 750 | ns |
| | | after falling edge of pin DRIVER | 1.8 | 2.2 | 2.6 | µs |
| $V_{opc(ISENSE)}$ | overpower compensation voltage on pin ISENSE | $I_{AUX}$ = −0.3 mA | 700 | 765 | 830 | mV |
| | | $I_{AUX}$ = −1.46 mA | 400 | 450 | 500 | mV |

**Table 7. Characteristics**...*continued*

*$T_{amb}$ = 25 °C; $V_{CC}$ = 20 V; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{opp(ISENSE)}$ | overpower protection voltage on pin ISENSE | counter trigger level | | | | |
| | | $I_{AUX}$ = −0.3 mA | 450 | 500 | 550 | mV |
| | | $I_{AUX}$ = −1.46 mA | 265 | 295 | 325 | mV |
| $t_{d(opp)}$ | overpower protection delay time | start-up mode; $V_{CTRL}$ > 5 V | 36 | 40 | 44 | ms |
| | | normal mode | 180 | 200 | 220 | ms |
| $t_{d(restart)}$ | restart delay time | | 720 | 800 | 820 | ms |
| **Overvoltage protection (pin AUX)** | | | | | | |
| $V_{ovp(AUX)}$ | overvoltage protection voltage on pin AUX | | 2.88 | 3 | 3.12 | V |
| $t_{det(ovp)}$ | overvoltage protection detection time | in the secondary stroke | 1.9 | 2.3 | 2.7 | µs |
| **Temperature protection** | | | | | | |
| $T_{pl(IC)}$ | IC protection level temperature | | 130 | 140 | 150 | °C |

## 12 Application information

A power supply with TEA18363T is a flyback converter operating in QR mode or DCM (see Figure 3).

Capacitor $C_{VCC}$ buffers the IC supply voltage. The IC supply voltage is powered from the mains via D1, D2, $R_{HV}$ during start-up. It is powered via the auxiliary winding during normal operation. $R_{HV}$ defines the current into the HV pin for brownout detection and mains detection.

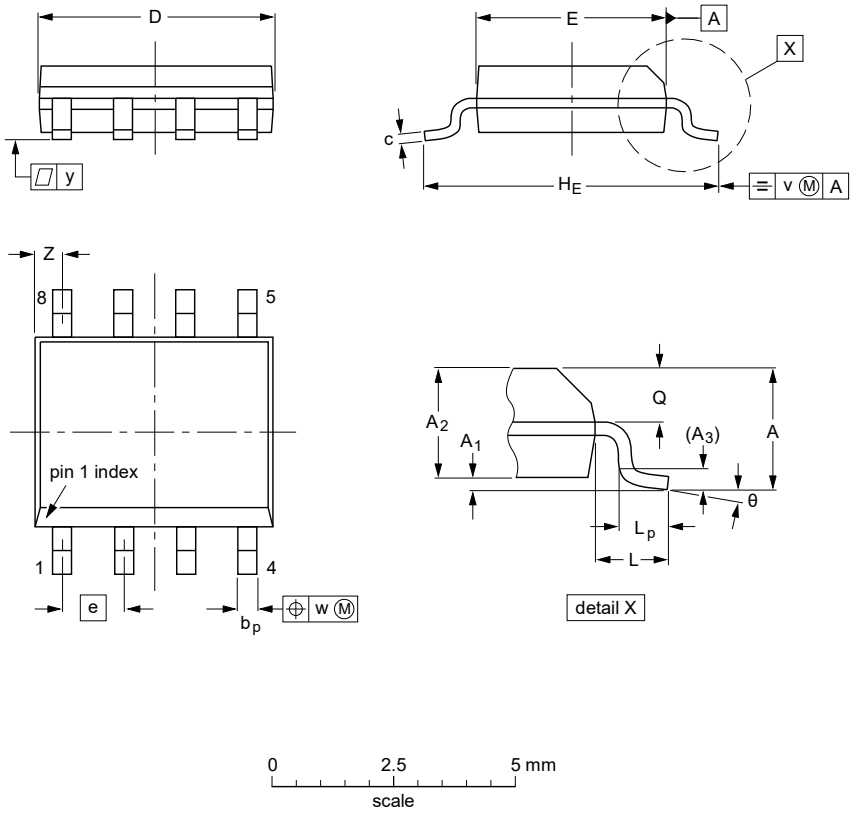
Sense resistor $R_{sense}$ converts the current through MOSFET S1 into a voltage on pin ISENSE. The value of $R_{sense}$ defines the maximum primary peak current through MOSFET S1. Resistor $R_{SS}$ and capacitor $C_{SS}$ define the soft start time.

Resistor $R_{DRIVER}$ is required to limit the current spikes to pin DRIVER because of parasitic inductance of the current sense resistor $R_{sense}$. $R_{DRIVER}$ also dampens possible oscillation of MOSFET S1. Adding a bead on the gate pin of MOSFET S1 can be required to prevent local oscillations of the MOSFET.

The resistor $R_{AUX2}$ determines the compensation for input voltage variation. The ratio of $R_{AUX1}$ and $R_{AUX2}$ determines the overvoltage protection at the AUX pin.

## 13 Package outline

**SO8: plastic small outline package; 8 leads; body width 3.9 mm** **SOT96-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 5.0<br>4.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | 8°<br>0° |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.20<br>0.19 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.024 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Notes**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT96-1 | 076E03 | MS-012 | | | | ~~99-12-27~~<br>03-02-18 |

**Figure 14. Package outline SOT96-1 (SO8)**

# 14 Revision history

**Table 8. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| TEA18363T/2 v.1 | 20230306 | Product data sheet | - | - |

# 15 Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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