



MC9S08AC60 Data Sheet Errata

by: Microcontroller Solutions Group

This errata document describes corrections to the *MC9S08AC60 Series Data Sheet*, order number MC9S08AC60. For convenience, the addenda items are grouped by revision. Please check our website at <http://www.freescale.com> for the latest updates.

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1 Errata for Revision 2

Table 1. MC9S08AC60 Rev 2 Errata

Location	Description
Section 4.4.3/Page 53	First sentence: Remove the sentence “Figure 4-2 is a flowchart for executing all of the commands except for burst programming”
Figure 4-2/Page 53	Replace Figure 4-2 with the following two figures: <pre> graph TD START((START)) --> ReadFCDIV[Read: FCDIV register] ReadFCDIV --> FDIVLD{FDIVLD Set?} FDIVLD -- yes --> ReadFSTAT1[Read: FSTAT register] FDIVLD -- no --> WriteFCDIV[Write: FCDIV register] WriteFCDIV --> ReadFSTAT1 ReadFSTAT1 --> FCBEF{FCBEF Set?} FCBEF -- no --> WriteFCDIV FCBEF -- yes --> FACCERR{FACCERR/FPVIOL Set?} FACCERR -- yes --> ClearFSTAT[Write: FSTAT register Clear FACCERR/FPVIOL 0x30] ClearFSTAT --> Step1[1. Write: Flash Array Address and Program Data] FACCERR -- no --> Step1 Step1 --> Step2[2. Write: FCMD register Program Command 0x20] Step2 --> Step3[3. Write: FSTAT register Clear FCBEF 0x80] Step3 --> ReadFSTAT2[Read: FSTAT register] ReadFSTAT2 --> FCCF{FCCF Set?} FCCF -- yes --> EXIT((EXIT)) FCCF -- no --> ReadFSTAT2 </pre> Example Program Command Flow

Table 1. MC9S08AC60 Rev 2 Errata (continued)

Location	Description
	<pre> graph TD START((START)) --> ReadFCDIV[Read: FCDIV register] ReadFCDIV --> FDIVLD{FDIVLD Set?} FDIVLD -- yes --> ReadFSTAT1[Read: FSTAT register] FDIVLD -- no --> WriteFCDIV[Write: FCDIV register] WriteFCDIV --> ReadFSTAT1 ReadFSTAT1 --> FCBEF{FCBEF Set?} FCBEF -- no --> ReadFSTAT1 FCBEF -- yes --> WriteFSTAT[Write: FSTAT register Clear FACCERR/FPVIOL 0x30] WriteFSTAT --> WriteFlash[1. Write: Flash Block Address and Dummy Data] WriteFlash --> WriteFCMD[2. Write: FCMD register Erase Verify Command 0x05] WriteFCMD --> WriteFSTAT2[3. Write: FSTAT register Clear FCBEF 0x80] WriteFSTAT2 --> ReadFSTAT2[Read: FSTAT register] ReadFSTAT2 --> FCCF{FCCF Set?} FCCF -- no --> ReadFSTAT2 FCCF -- yes --> FBLANK{FBLANK Set?} FBLANK -- yes --> EXIT1((EXIT Flash Block Erased)) FBLANK -- no --> EXIT2((EXIT Flash Block Not Erased)) </pre> Example Erase Verify Command Flow
Section 4.4.6/Page 55	First paragraph, fourth sentence: change from "...3-bit control field..." to "... 7-bit control field...." Remove the sentence "A separate control bit allows block protection of the entire FLASH memory array". Last sentence: change from "All seven of these control bits..." to "All eight of these control bits.."

Table 1. MC9S08AC60 Rev 2 Errata (continued)

Location	Description																																										
Table 15-8/Page 268	Replace Table 15-8 with the following table to show “Software compare only” configuration for the “Output compare” mode. Mode, Edge, and Level Selection <table><tr><th>CPWMS</th><th>MSnB:MSnA</th><th>ELSnB:ELSnA</th><th>Mode</th><th>Configuration</th></tr><tr><td>X</td><td>XX</td><td>00</td><td colspan="2">Pin is not controlled by TPM. It is reverted to general purpose I/O or other peripheral control</td></tr><tr><td rowspan="9">0</td><td rowspan="3">00</td><td>01</td><td rowspan="3">Input capture</td><td>Capture on rising edge only</td></tr><tr><td>10</td><td>Capture on falling edge only</td></tr><tr><td>11</td><td>Capture on rising or falling edge</td></tr><tr><td rowspan="4">01</td><td>00</td><td rowspan="4">Output compare</td><td>Software compare only</td></tr><tr><td>01</td><td>Toggle output on channel match</td></tr><tr><td>10</td><td>Clear output on channel match</td></tr><tr><td>11</td><td>Set output on channel match</td></tr><tr><td rowspan="2">1X</td><td>10</td><td rowspan="2">Edge-aligned PWM</td><td>High-true pulses (clear output on channel match)</td></tr><tr><td>X1</td><td>Low-true pulses (set output on channel match)</td></tr><tr><td rowspan="2">1</td><td rowspan="2">XX</td><td>10</td><td rowspan="2">Center-aligned PWM</td><td>High-true pulses (clear output on channel match when TPM counter is counting up)</td></tr><tr><td>X1</td><td>Low-true pulses (set output on channel match when TPM counter is counting up)</td></tr></table>	CPWMS	MSnB:MSnA	ELSnB:ELSnA	Mode	Configuration	X	XX	00	Pin is not controlled by TPM. It is reverted to general purpose I/O or other peripheral control		0	00	01	Input capture	Capture on rising edge only	10	Capture on falling edge only	11	Capture on rising or falling edge	01	00	Output compare	Software compare only	01	Toggle output on channel match	10	Clear output on channel match	11	Set output on channel match	1X	10	Edge-aligned PWM	High-true pulses (clear output on channel match)	X1	Low-true pulses (set output on channel match)	1	XX	10	Center-aligned PWM	High-true pulses (clear output on channel match when TPM counter is counting up)	X1	Low-true pulses (set output on channel match when TPM counter is counting up)
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2 Revision History

Table 2 provides a revision history for this document.

Table 2. MC9S08AC60AD Revision History

Rev. Number	Substantive Changes	Date of Release
0	Initial release	11/2009

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