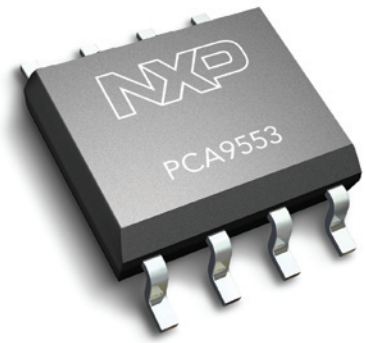

NXP 2/4/8/16-bit I²C/SMBus LED blinkers PCA9550/51/52/53

LED blinking with GPIO expansion

These I²C/SMBus-compatible GPIO expanders, optimized for blinking in LED-status applications, support two user-programmable blink rates, without overloading the I²C-bus or tying up the I²C-bus master.

Key features

- Compatible with I²C-bus and SMBus
- Two user-programmable blink rates and duty cycles
  - Blink rate: 0.025 to 6.4 sec (40 to 0.156 Hz)
  - Duty cycle: 0.4 to 100%
- Internal oscillator accurate to ±10% and requires no external components
- Open-drain outputs can drive LEDs directly (25 mA max sink per bit)
- High maximum device limits (50, 100, or 200 mA)
- I/O states readable via I²C/SMBus
- Any bit not used to drive an LED can be used as normal GPIO
- Active-low hardware reset saves power and simplifies design
- Low standby current (I_{STB}): 1.5 µA (max)
- Operating voltage: 2.3 to 5.5 V
- All I/O tolerant to 5.5 V
- Temperature range: -40 to +85 °C
- I²C-bus clock frequency: 0 to 400 kHz
- ESD protection exceeds JEDEC standards
- High-volume CMOS process
- Package options: SO, TSSOP, HVQFN

Applications

- LED status

The NXP PCA9550, PCA9551, PCA9552, and PCA9553 are used to blink LEDs in I²C-bus and SMBus applications. Each LED can be on, off, or flashing at one of two programmable rates without overloading the I²C-bus or tying up the I²C-bus master.

The blink rate can vary from 0.025 to 6.4 seconds (40 to 0.156 Hz) in 256 steps. The duty cycle is programmable in 256 steps, for flexible on and off times. There can be a short flash of light, for example, or long on periods with a very short off period.

Any bits that aren't used to control LEDs can be used as general-purpose I/O (GPIO), for a quick, easy to add sensors, push-buttons, alarm monitors, LEDs, fans, and more.

On the PCA9551 and PCA9552, three hardware pins (A0, A1, A2) let up to eight identical devices share the same I²C/SMBus. On the PCA9550, a single hardware pin (A0), supports up to two devices on the same I²C/SMBus. Due to hardware pin limitations, the PCA9553 doesn't have address pins so the address is fixed.

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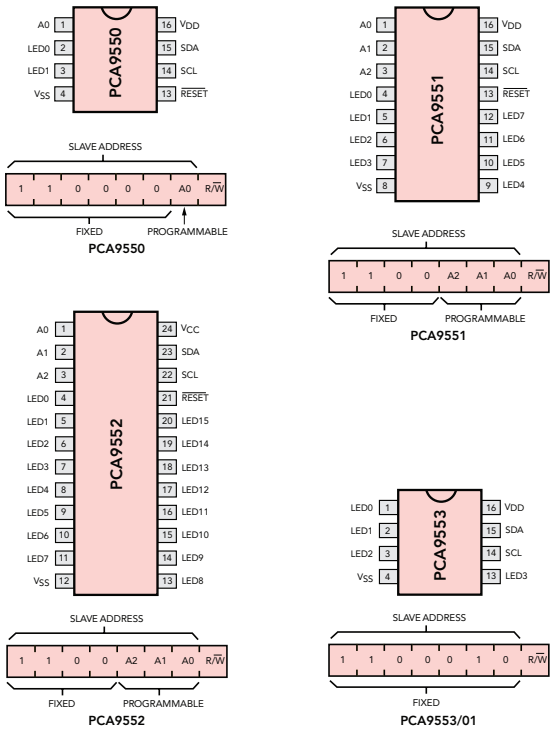
Each device features open-drain outputs that sink 25 mA per bit. The PCA9550 supports a maximum of 50 mA, the PCA9551 and PCA9553 a maximum of 100 mA, and the PCA9552 a maximum of 200 mA (100 mA per 8-bit group).

On the PCA9550, PCA9551, and PCA9552, an external active-low reset hardware pin ($\overline{\text{RESET}}$) returns registers to their default states, without having to cycle power to the equipment, if the I²C-bus locks up.

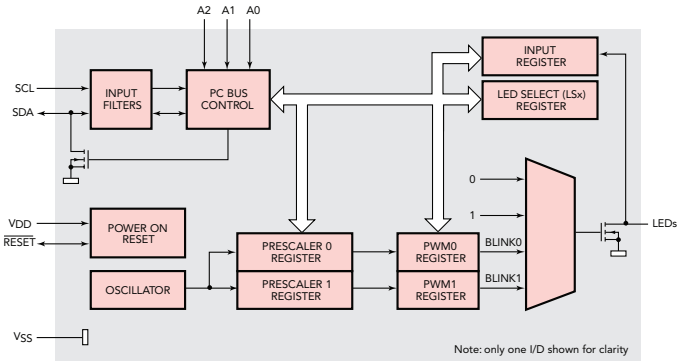
ESD protection exceeds 2000 V HBM per JESD22-A114, 150 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101. JESDEC Standard JESD78 latch-up testing exceeds 100 mA.

Except for the number of bits and address pins, the functional diagram and I/O schematic are the same for all of the devices.

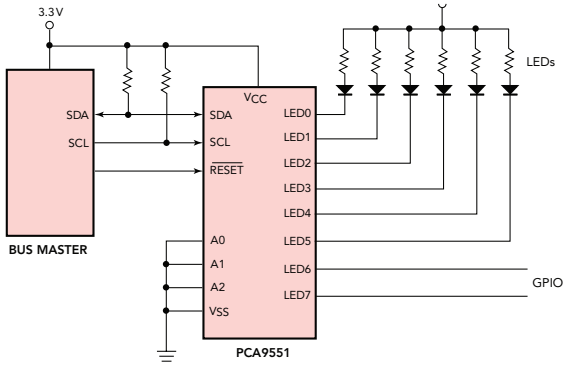
More information on NXP LED blinkers can be found in application note AN264.



Pin configuration



Block diagram



Typical application

Order information

Package	Container	PCA9550	PCA9551	PCA9552	PCA9553/01
SO	Tube T & R	PCA9550D PCA9550D-T	PCA9551D PCA9551D-T	PCA9552D PCA9552D-T	PCA9553D/01 PCA9553D-T/01
TSSOP	Tube T & R	PCA9550DP-T	PCA9551PW PCA9551DP-T	PCA9552PW PCA9552DP-T	PCA9553DP/01-T
HVQFN	T & R		PCA9551BS-T	PCA9552BS-T	

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