Application Note

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Migrating from the MC68302 to the MCF5272

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Leveraging the widespread industry success of Freescale's 68K family, the ColdFire® architecture is designed specifically to provide higher performance in embedded applications at a lower cost. Since the ColdFire architecture stems from the Freescale 68000 architecture, it allows designers to take advantage of the established tool support, code evolution, and engineering expertise.

This architectural relationship encourages users to migrate from 68K to ColdFire, the next high-performance generation of the 68K family of processors. This application note describes what designers and programmers should consider when migrating from the MC68EN302 and its derivatives to the MCF5272 microprocessor. For additional information about the MCF5272, refer to the *MCF5272 User's Manual* (MCF5272UM/D).

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1.1 Comparison

1.1.1 Advantages and Challenges of Migration

This section highlights the various advantages and challenges involved when migrating from the MC68302 to the MCF5272.

The MCF5272 provides a higher level of performance while maintaining many characteristics of the MC68302's architecture. Following is a list of the advantages of migrating to the MCF5272:

- More cost-effective
- Provides a higher level of integration
- Uses 32-bit address and data paths

- Supports the M68000 instruction set via an emulation library
- Builds on the established tool support of the MC68302
- Represents the future ColdFire migration path

Following is a list of differences that may present challenges in migrating from the MC68302 to the MCF5272:

- Different operating voltages
- Differences in capacitive loading
- Different pinout/package
- No MCF5272 external master support
- No Communications Processor Module (CPM) on the MCF5272

See Section 1.2, “Hardware Considerations,” for information on addressing these differences.

1.1.2 Summary and Feature Comparison Tables

Although this document focuses primarily on the migration from the MC68EN302 to MCF5272, Table 1 includes information comparing some of the features of the other various MC68302 derivatives.

Table 1. MCF5272 and MC68XX302 Comparison

	MCF5272	MC68EN302	MC68302	MC68LC302
Voltage	3.3V	5V	5V, 3.3V	5V, 3.3V
Frequency	66MHz	20, 25MHz	16, 20, 25, 33	16, 20, 25
Performance	63MIPS	1.6MIPS	2.1MIPS	1.6MIPS
Package	196-pin MAPBGA	144-lead LQFP	132-lead PQFP 144-lead LQFP 132-lead PGA	100-lead LQFP
Core	V2 ColdFire	68000 core	68000 core	Static EC000
Debug	ColdFire Rev A BDM Module, JTAG	JTAG	—	—
Chip Selects	8 chip selects	4 chip selects	4 chip selects	4 chip selects
DRAM	SDRAMC–1 bank	ADRAMC–2 banks	—	—
DMA	1 channel	7 channels	6 channels	4 channels
Serial Communication	2 UARTs	3 SCCs	3 SCCs	2 SCCs
	PLIC (IDL/GCI)	2 SMCs	2 SMCs	2 SMCs
	QSPI	SCP	SCP	SCP
Ethernet	10/100 Ethernet	10Mbps ethernet	—	—
Other Modules	4 timers	2 timers	2 timers	2 timers
	USB	—	—	—
	GPIOs	GPIOs	GPIOs	GPIOs

1.2 Hardware Considerations

1.2.1 Voltage Conversion

One important consideration in migrating from the MC68302 to the MCF5272 is the difference in voltage. The MC68302 is a 5V device while the MCF5272 is a 5V-tolerant 3.3V device. Although the MCF5272 is 5V-tolerant, the use of 5V devices with the MCF5272 is not recommended. The output high voltage (V_{OH}) minimum specification for the MCF5272 is 2.4V, so any 5V device that is connected directly to the MCF5272 should have a input high voltage (V_{IH}) minimum spec 2.4V or lower to be compatible with the MCF5272's logic levels. Secondly, unless all of the devices on the MCF5272's local bus are 5V tolerant, the 5V devices will need to be isolated from the bus to ensure that these devices are not damaged. Refer to Figure 1 for an example of how buffers can be used to isolate 5V memories and peripherals from a 3.3V bus.

1.2.2 Driver Strength/Capacitive Loading

Another issue to take into consideration when migrating from the MC68302 to the MCF5272 is the drive capability of the parts. Whereas the majority of MC68302 specifications assume a 130pF loading on the pin, the MCF5272 tolerates loading up to 30pF. In many systems, external buffers will be needed to reduce the loading on the MCF5272 bus. Figure 1 shows a possible buffering scheme that can be used to reduce loading.

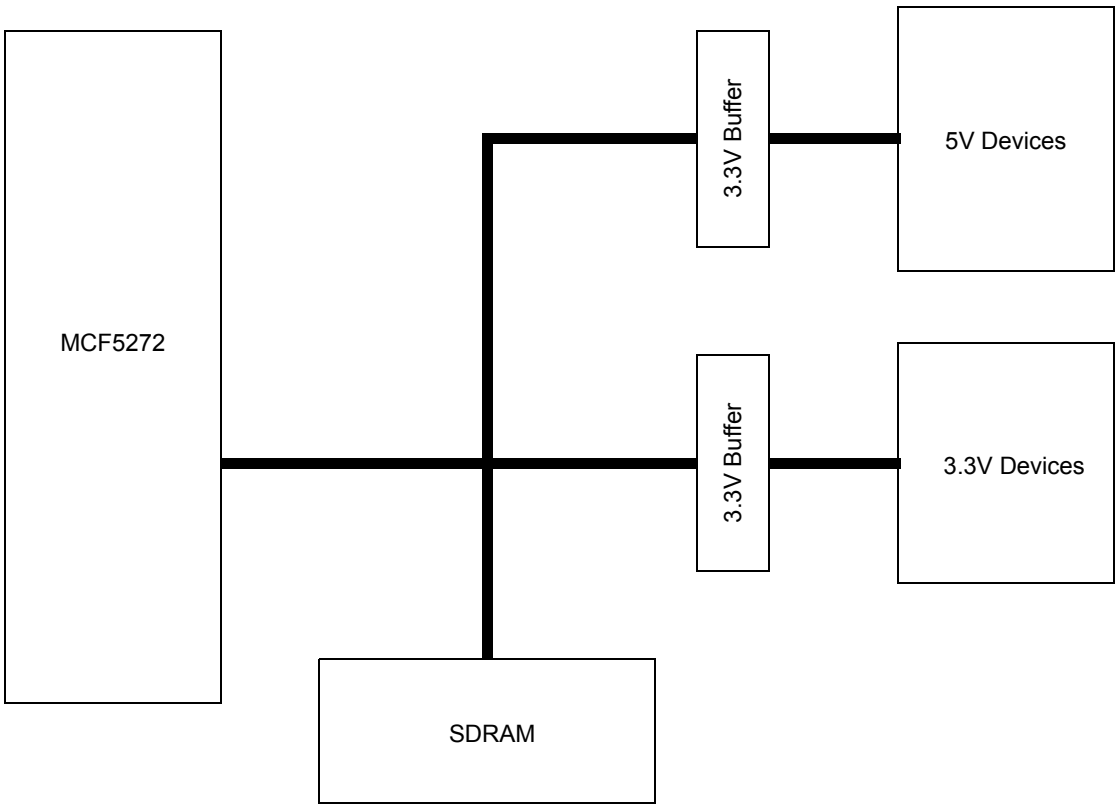

Figure 1. Buffering Scheme for Isolating 5V Memories and Peripherals on a 3.3V Bus

1.2.3 Frequency and Performance

One of the primary advantages of migrating to the MCF5272 is the significant increase in performance and frequency. Whereas the MC68302 has a Dhrystone 2.1 MIPS rating of approximately 5.6 MIPS when running at 33MHz, the MCF5272 offers approximately 31 MIPS of performance at the same frequency. That is, the MCF5272 offers close to a 6x performance boost without changing the bus frequency. Moreover, the MCF5272 can provide 63 MIPS performance at its maximum frequency of 66MHz.

1.2.4 Operating the MCF5272 in 16-bit Data Bus Mode

Unlike the MC68302, the MCF5272 has a 32-bit data bus. In order to maintain as much compatibility as possible with the MC68302, customers can choose to operate the MCF5272 in a 16-bit data bus mode. The 16-bit data bus mode is selected by the state of the QSPI_Dout/WSEL pin during reset. Driving the signal low selects the standard 32-bit mode, and driving the signal high selects the 16-bit data bus mode. When operating in the 16-bit data bus mode, the unused data pins are available as GPIOs.

1.2.5 Signal Mapping

Refer to Appendix A, “Signal Mapping” for a table correlating MC68302 and MCF5272 signals.

1.2.6 Module Comparisons

1.2.6.1 MCF5272 SDRAMC vs. MC68EN302 DRAMC

The most significant difference between the devices’ DRAM controllers (DRAMC) is that the MCF5272 supports SDRAM and the MC68EN302 supports ADRAM. Therefore, customers migrating from the MC68EN302 should replace their current system’s DRAM with SDRAM. Switching to SDRAM can be beneficial since ADRAM is becoming increasingly harder to procure and does not offer performance comparable to SDRAM.

The other notable difference between the controllers is that the MCF5272 can only access one bank of memory while the MC68EN302 provides support for up to two banks of memory. This could cause problems for applications that require very large amounts of DRAM. However, the MCF5272 can support up to 32MBytes of SDRAM, so in most cases, the one bank of SDRAM on the MCF5272 can support enough memory to be compatible with the two banks of DRAM available on the MC68EN302.

1.2.6.2 DMA Module Differences

The MCF5272 DMA is a basic module that lacks some of the functionality available on the MC68302’s IDMA. In particular, the MCF5272 does not have any external request pins ($\overline{\text{DREQ}}$, $\overline{\text{DACK}}$, and $\overline{\text{DONE}}$). If external requests are required, one possible workaround is to use an external interrupt signal as a DMA request. When the interrupt line is asserted, then the interrupt handler can be used to program and start the DMA transfer.

In addition, the MCF5272’s DMA controller does not support the cycle steal mode DMA transfer capability found on the MC68302. A possible workaround is to use many small DMA transfers instead of one large one transferred in small increments. However, as the transfers get smaller, the overhead associated with setting up the DMA begins to make this solution impractical. In this case, it is better to transfer the data using software instead of the DMA.

1.2.6.3 Ethernet Module

The MCF5272 and the MC68EN302 both have on-chip ethernet MACs. The controller on the MC68302 is older and can only support the original 10Mbps 7-wire interface. The MCF5272 adds support for 100Mbps and 10Mbps MII communication as well as the 10Mbps 7-wire interface.

The function and programming of the ethernet controllers on the MCF5272 and MC68EN302 are similar, but the buffer descriptors are handled differently on the two devices. The MC68302 has on-chip buffer descriptor RAM that is used to store the descriptors. The allocation of the memory between the receive and transmit buffers is controlled by the EDMA[BDSIZE] field. The MCF5272 ethernet controller implementation uses external (off-chip) buffer descriptors where the R_DES_START and X_DES_START registers are pointers to the external memory used for the descriptors. Because the buffer descriptors are stored in external memory, the ethernet controller requires more time to access them than buffer descriptors stored in internal memory; however, the queue size for external buffer descriptors can be much larger. The last entry in the circular buffer descriptor queue is designated by setting the [W] bit in the descriptor. The fact that more data can be transferred with less CPU intervention allows for 100Mbps operation. Due to the changes in how the buffer descriptors are handled, the MCF5272 eliminates the ethernet DMA configuration status register (EDMA), and implements some slight changes in the buffer descriptor definitions.

The interrupt functions of the MCF5272's ethernet module are very similar to those implemented on the MC68302. Though the majority of interrupt events are the same, the location of the interrupt event bits (and the corresponding mask bits) have moved, so the code that tests for different interrupt conditions will need to be updated in most cases. The following list outlines differences between the devices' interrupt events.

- The MCF5272 does not have a back off done interrupt.
- The MCF5272 does not have a BSY (busy) interrupt.
- The MCF5272 has an additional interrupt event for MII communication.

1.2.6.4 SCC vs. UART

The MCF5272 has two UART modules that provide full-duplex asynchronous/synchronous receiver and transmitter functionality in either normal or multidrop modes. The MCF5272's UART has a subset of the functionality of the MC68302's Serial Communication Controllers (SCCs). The most notable difference is that the MCF5272 works only on a character basis. Since the MCF5272 only supports transfer of individual characters, there are no buffers or buffer descriptors associated with the UART.

1.2.6.5 SCP vs. QSPI

The MC68302's Serial Communication Port (SCP), using a subset of Motorola's Serial Peripheral Interface (SPI), can communicate with a variety of serial devices. The major differences between the SCP and the Queued Serial Peripheral Interface (QSPI) implemented on the MCF5272 are in the QSPI's queue and interrupt capabilities.

The QSPI can queue up to 16 words of data for transmission without CPU intervention (allowing CPU bandwidth to be allocated elsewhere). QSPI successive transmissions can occur back-to-back whereas the SCP has a minimum delay of 2-8 bit times, depending on the SCP clock rate.

The SCP has no interrupt capabilities, while the QSPI has the following interrupt sources:

- QSPI finished interrupt (SPIF), which is asserted when the QSPI has completed all of the commands in the queue

- Abort interrupt (ABRT), which indicates that the QSPI enable bit in the QSPI delay register has been cleared by a user write rather than by the QSPI's completion of the command queue
- Write collision error flag (WCEF), which indicates that an attempt has been made to write to the RAM entry that is currently being executed

In considering the differences between SCP and QSPI functionality, some other differences should be taken into account. The QSPI does not have a Loop Mode, which is useful for local diagnostic functions, like the SCP. The MC5272's CPU cannot access QSPI RAM. A user can only access it indirectly via the QSPI address register (QAR) and the QSPI data register (QDR). The SCP can only have clock rate of up to 4.096 MHz, while the QSPI can have a clock rate of up to 33MHz.

1.2.6.6 SCC/SCM vs. PLIC

The primary difference between the SCC/SCM and the Physical Layer Interface Controller (PLIC) modules is the number of Integrated Service Digital Network (ISDN) channels each can support. The MC68302 requires SCC 1, 2, 3 and SMC 1, 2 to be time multiplexed together in order to provide one Basic Rate, 2B+D interface. In this scenario, the SCCs/SMCs cannot simultaneously function as a UART or anything else. On the other hand, the MCF5272 PLIC is its own separate module with 4 ports, each of which supports a Basic Rate Interface.

Another difference between the SCC/SCM and the PLIC is that the SCC/SCM supports only slave mode and 10-bit Inter Digital Link (IDL). The PLIC supports both master and slave mode, and both 10- and 8-bit IDL. However, the PLIC does not support output serial data strobes, which allow the selection of either or both B1 and B2 channels available on the SCC/SCM. Table 2 shows the correlation of pins associated with the SCC/SCM and the PLIC modules.

Table 2. SCC/SCM and PLIC Pin Comparisons

MC68302	MCF5272
L1CLK	DCL
L1TxD	Dout
L1RxD	Din
L1SY1	FSC
L1RQ	DREQ
L1GR	DGNT
SDS1	N/A
SDS2	N/A

1.2.6.7 SCC vs. Soft HDLC

The primary difference between the MC68302's SCC and the MCF5272's soft HDLC (High-level Data Link Control) is that one is a hardware implementation and the other is a software implementation. The hardware implementation offers more functionality than the software implementation, but there is also more complexity in its use. The soft HDLC, implemented as a framer/deframer function, is available as an object format library ready for linking with user code via a simple Application Programmer's Interface (API).

Another difference between the SCC and soft HDLC is that each supports different data rates. The SCC, at 16.67 MHz, was initially designed to handle a data rate of 256 Kbps, though it can actually achieve 1.8Mbps on one SCC. At this frequency, the MC68302 can support data rates of 74 Kbps on the remaining two SCCs

(SCC 2 and 3). At most, the SCC can support 3 HDLC channels. Though the MCF5272 can support several instantiations of the soft HDLC module, each supporting one channel, it can only operate at 56 or 64 Kbps.

Whereas the SCC supports Synchronous Data Link Control (SDLC) (though not the loop mode of this protocol), the soft HDLC does not support SDLC. A wrapper application would have to be written on top of the soft HDLC to implement the loop and hub go-ahead modes. The wrapper application should handle the maintenance of all connected channels' intermediate status.

The following list outlines other differences between the soft HDLC module and the SCC:

- The MCF5272's cyclic redundancy check (CRC) is a 16-bit calculation, but the SCC's CRC can be either 16- or 32-bit.
- The CRC calculation is optional for both when transmitting; however, when receiving, the soft HDLC can disable CRC checking while the MC68302 cannot. The soft HDLC can simply ignore the CRC if the calculation is not needed.
- The soft HDLC has address recognition of up to three independent addresses per channel: two regular independent addresses, one independent address associated with a mask, and the broadcast address; the SCC has five registers for address recognition: one mask register and 4 address registers.
- The SCC has an event register that reports HDLC channel events and generates interrupts. Although the soft HDLC can keep track of various events, it cannot generate interrupts based on those events.
- The SCC uses buffer descriptors in either internal dual port RAM or external memory for storing data associated with each SCC. It also keeps track of some status information about the buffer. The soft HDLC does not have these capabilities.

1.3 Software Considerations

1.3.1 Mapping 24-bit MC68302 Addresses to the 32-bit MCF5272

The fact that the MCF5272 supports 32-bit addressing and the MC68302 supports 24-bit addressing should make no difference when porting the system software because the MCF5272 can use a 24-bit addressing scheme. This is accomplished by treating the upper 8-bits as a "don't-care" (except when using on-chip cache). The MCF5272 has three registers that control how specific regions of address space are assigned access control attributes: two access control registers (ACR0 and ACR1) and the cache control register (CACR). Since the ACRs and the CACR use address bits 31–24 to define reference attributes for memory regions, virtual-to-physical memory mapping can be used to map unique 24-bit address space regions to unique 16-Mbyte regions in the 32-bit address space. This will enable certain areas of the physical memory map to utilize the capabilities of MCF5272 caching. For instance, this can be accomplished by concatenating A[31:24] = $01 in front of the first 24-bit address region, and using ACR0 to control the caching scheme for this region. This can also be done for ACR1 and CACR to configure cacheable memory regions. For more details, please refer to chapter 4, "Cache," of the MCF5272 User's Manual.

1.3.2 Read-Modify-Write (RMW) Cycles

If the original MC68302 code uses the Test And Set (TAS) instruction for implementing the locked or read-modify-write transfer sequence in hardware, the instruction must be emulated in software on the

MCF5272. In order to do this, the interrupt mask should be raised to level 7, the read, modify, and write instructions should be executed, and then the mask should be lowered back down to the appropriate level. Performing this sequence of instructions will guarantee that they will execute uninterrupted with the exception of a level 7 interrupt, which is nonmaskable.

1.3.3 Cache Coherency

Cache coherency is the term used to describe the consistency (or coherency) of on-chip cache and external memory, if other masters use the same memory. It is primarily an issue when cache is used in copyback mode and a second bus master in the system modifies a shared piece of memory. This creates a mismatch between the data stored in the cache and the external memory. However, since the MCF5272 does not support secondary bus masters, cache coherency is not a problem.

1.3.4 Porting from M68000 Family Devices

For a detailed explanation of porting from M68000, please refer to Appendix B of the MCF5206e User's Manual.

1.4 Debug Support/3rd Party Tools

As processors become faster and more powerful, developing and debugging applications becomes a more difficult task. Although in-circuit emulation is a powerful technique, it can be relatively expensive or impractical as CPU complexity increases. Motorola's Background Debug Mode (BDM), found in the MCF5272, incorporates debugging circuitry to provide the user with access and control via a small number of dedicated pins and an inexpensive connector.

BDM easily provides the functionality needed to start/stop the target, step through the program, and read/write target memory and registers. When controlled by a debugger, this provides a very powerful means of developing code for embedded processors.

The MC68302, which does not have BDM, uses the Application Development System (ADS) and Application Development Interface (ADI) for debugging purposes. While the ADS board requires that an ADI board be installed into one of the host's expansion slots in order to be effective, the BDM utilizes a simple parallel port (which already exists on most hosts) to establish communications for debugging.

For a list of third-party tool vendors that support the MCF5272, please refer to http://mot.com/coldfire.

1.5 Packaging

With the trend toward miniaturization, smaller, lighter, and higher performance products have paved the way for smaller component packages and higher pin counts. For this reason, the Mold Array Process-Ball Grid Array (MAPBGA) is used as the production package for the MCF5272. It is a surface mount package that uses solder balls arranged in a grid array instead of the lead pins normally used in Quad Flat Pack (QFP) and other packages. The MCF5272's 196-pin MAPBGA package gives it many advantages over a QFP.

The most evident advantage of the MAPBGA versus the QFP is the savings in board real estate. Most BGAs are typically 20-25% smaller than their QFP counterparts. For the MAPBGA package, the entire surface of the die, rather than just the edges, can be used for interconnection. When the total board area required to place and route the package is taken into account, the MAPBGA can reduce size by as much as 50%. Figure 2 shows the differences between the QFP and the MAPBGA.

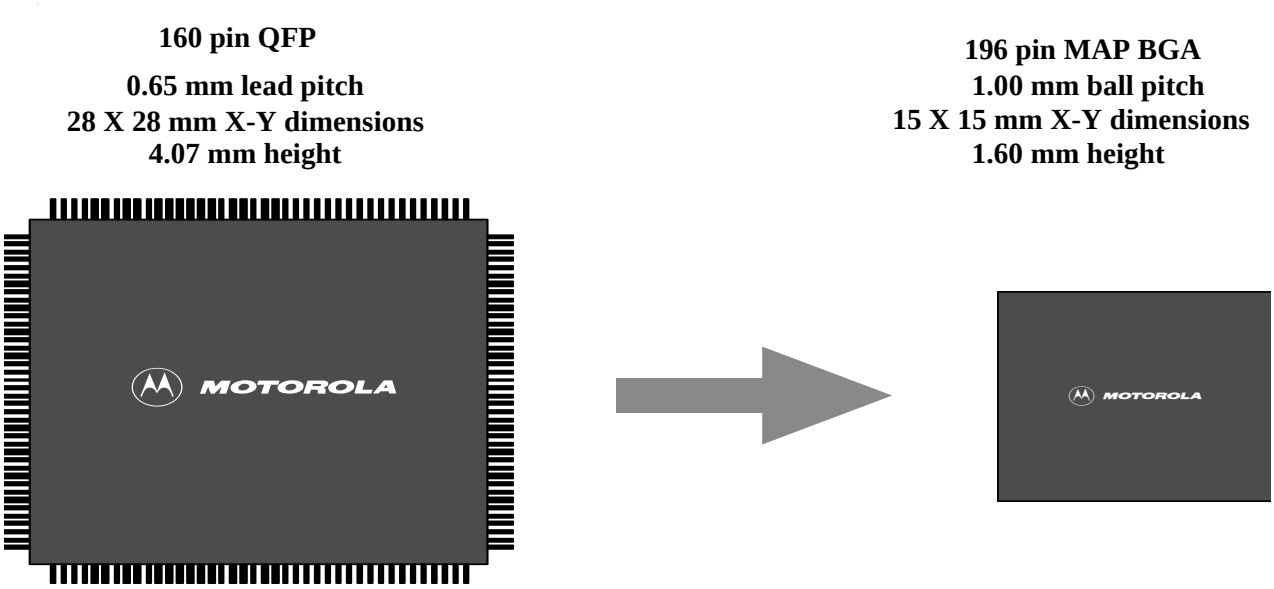

Figure 2. Customer Board Area Reduction Example

Lead pitch is a major consideration when working with high pin count QFPs. For these packages, the lead pitch can be as fine as 0.50 mm. The BGA package with the same number of pins is easier to mount, since the lead pitch is wider than a QFP package. BGAs are also less fragile and easier to handle both before and during assembly. The placement operation for this package is usually far easier and more reliable than for fine-pitch QFPs.

BGAs also have higher assembly yields. For example, BGAs typically have less than 5 parts per million joints (ppmj) compared to the 50–100 ppmj of QFP devices. BGAs have higher assembly yields than QFPs for the following reasons:

- No bent leads or coplanarity problems
- Self-aligning on solder pads
- Solder balls are always solderable (unlike plated leads)
- Easy solder paste printing
- Large pitch: 1.0 mm, 1.5 mm, 1.27 mm
- Large ball diameter sizes: MAPBGA 19.68 mils

In general, BGAs have better electrical and thermal properties than their QFP counterparts. The long fingers of the QFP lead frame make it more inductive than shorter ones. Additional enhancements can be made to the BGA package by adding metal layers for power and ground.

Appendix A
Signal Mapping

Table 3 lists the signal mappings for each signal function.

Table 3. MCF5272 and MC68302 Signal Mapping

MC68302	MC68EN302	MCF5272
Clocks		
EXTAL	EXTAL	CLKIN
XTAL	XTAL	—
CLKO	CLKO	—
System Control		
$\overline{\text{RESET}}$	—	$\overline{\text{RSTI}}$
$\overline{\text{HALT}}$	—	—
$\overline{\text{BERR}}$	—	—
BUSW	—	—
DISCPU	—	—
$\overline{\text{FRZ}}$	—	—
—	—	$\overline{\text{DRESETEN}}$
—	—	$\overline{\text{RSTO}}$
—	—	$\overline{\text{HIZ}}$
Address Bus		
A[23:0]	A[23:0]	A[22:0]
Data Bus		
D[15:0]	D[15:0]	D[31:0]
Bus Control		
$\overline{\text{AS}}$	—	
R/W	—	R/W
	—	$\overline{\text{OE}}$
$\overline{\text{UDS}}$, $\overline{\text{LDS}}$	—	$\overline{\text{BS}}$[3:0]
$\overline{\text{DTACK}}$	—	$\overline{\text{TA}}$
$\overline{\text{RMC}}$/IOUT1	—	
IAC	—	
$\overline{\text{BCLR}}$	—	
Chip Selects		
$\overline{\text{CS}}$[3:0]	—	$\overline{\text{CS}}$[7:0]

Table 3. MCF5272 and MC68302 Signal Mapping (continued)

MC68302	MC68EN302	MCF5272
Bus Arbitration		
$\overline{BR}$	—	— [1]
$\overline{BG}$	—	
$\overline{BD}$	—	
Interrupts		
$\overline{IPL0}/\overline{IRQ1}$	—	INT[6:1]
$\overline{IPL1}/\overline{IRQ6}$	—	
$\overline{IPL2}/\overline{IRQ7}$	—	
IACK[1,6,7]	—	
AVEC	—	—
FC[2:0]	—	—
Timers		
TIN[1:0]	—	TIN[1:0]
TOUT[1:0]	—	TOUT[1:0]
WDOG	—	—
DMA		
$\overline{DREQ}$	—	— [2]
$\overline{DACK}$	—	
$\overline{DONE}$	—	
SDRAMC		
—	$\overline{RAS}$[1:0]	$\overline{RAS0}$
	$\overline{CAS}$[1:0]	$\overline{CAS0}$
	—	SDCLK
	$\overline{DRAMRW}$	$\overline{SDWE}$
	—	SDCLKE
	—	SDBA[1:0]
	—	A10_PRECHG

Table 3. MCF5272 and MC68302 Signal Mapping (continued)

MC68302	MC68EN302	MCF5272
Ethernet		
—	TCLK	E_TxCLK
	TX	E_TxD[3:0]
	CLSN	E_COL
	RENA	E_RxDV
	RCLK	E_RxCLK
	RX	E_RxD[3:0]
	TENA	E_TxEN
	—	E_RxER
		E_MDC
		E_MDIO
		E_TxER
		E_CRS
UART		
RXD	—	URT_RxD
TXD	—	URT_TxD
RCLK	—	URT_CLK
TCLK	—	
BRG	—	
$\overline{\text{CTS}}$	—	$\overline{\text{URT\_CTS}}$
$\overline{\text{RTS}}$	—	$\overline{\text{URT\_RTS}}$
$\overline{\text{CD}}$	—	—

1 The MCF5272 does not support external bus masters, so there are no external bus arbitration signals.
2 The MCF5272 does not support external DMA requests.

1.6 Document Revision History

Table 4 provides a revision history for this application note.

Table 4. Document Revision History

Rev. No.	Substantive Change(s)	Date of Release
0	Initial release.	February 2003

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