6/18/90

MC68302 SOFTWARE PERFORMANCE

The software performance of the MC68302 is the number of frames per second that can be transferred. This is a very different calculation from the number of bits per second that the SCCs can transmit as it involves the execution of code by the M68000 core together with the SCCs.

Experiments have been performed using two ADS302 boards to determine the software performance. Each board contains 1 MC68302 operating at 16.67 MHz, and 512K bytes of one waitstate DRAM, with all code executed out of 3 waitstate EPROM. The two boards passed frames (created and stored in DRAM) to each other with either 1 or all 3 SCCs operating. Each SCC was configured as a full-duplex HDLC channel.

The software running on each board consisted of different tasks, that communicate with message passing, along with the real-time kernel EDX. The varying results between entries is attributed to whether the software or the physical line is the performance bottleneck. If the result is close to the theoretical limit, the line is clearly the bottleneck. Since the amount of code executed is virtually the same regardless of the frame length and the number of SCCs used, the software limit is the highest value shown in the set of tables.

Layer 2 Experiments

Layer 7 - File Transfer Application
Layer 2 - LAPD or LAPB (1988 Blue Book compatible)
Layer 1 - MC68302 Chip Drivers
EDX - Real-time Kernel

One SCC Operating				
Serial Bit Rate	Frame Length	Window Size	I Frames/sec	TH-Lim
64 Kbps	30 bytes	3 frames	412	533
64 Kbps	256 bytes	3 frames	60	62
500 Kbps	30 bytes	3 frames	470	4167
500 Kbps	256 bytes	3 frames	365	488
500 Kbps	30 bytes	7 frames	875	4167
500 Kbps	30 bytes	9 frames	890	4167

Three SCCs Operating				
Serial Bit Rate	Frame Length	Window Size	I Frames/sec	TH-Lim
64 Kbps	30 bytes	3 frames	590	1600
500 Kbps	256 bytes	3 frames	566	1465

NOTES FOR LAYER 2 TABLES:
1. TH-Lim is the theoretical limit of the line assuming no overhead (such as flags, CRCs, zero insertion, and RR frames) and an infinite window size.
2. The window size (also known as k) is the number of frames that may be sent without receiving an acknowledgement (modulo 128). This value can impact performance considerably.
3. Only layer 2 information frames are counted in the total shown. The rate shown is the total full-duplex channel rate. Thus 890 I frames/sec is 445 transmitted and 445 received I frames/sec.
4. The frame length shown is an average value, and is defined as all bytes between the opening flag and the first CRC byte.
5. The layer 7 file transfer facility is not as extensive as a full layer 7 product such as FTAM.
6. Performance numbers for LAPB or LAPD are virtually the same.

Layer 3 Experiments

Layer 7 - File Transfer Application
Layer 3 - X.25 (1988 Blue Book compatible)
Layer 2 - LAPB (1988 Blue Book compatible)
Layer 1 - MC68302 Chip Drivers
EDX - Real-time Kernel

One SCC Operating					
Serial Bit Rate	Frame Length	L2 Window	L3 Window	I Frames/sec	TH Limit
500 Kbps	30 bytes	7 or 9	9	520	4167

NOTES FOR LAYER 3 TABLE:
1. TH-Lim is the theoretical limit of the line assuming no overhead (such as flags, CRCs, zero insertion, and RR frames) and an infinite window size.
2. The window size (also known as k and w) is the number of frames that may be sent without receiving an acknowledgement (modulo 128).
3. Only layer 2 information frames are counted in the total shown. The rate shown is the total full-duplex channel rate. Thus 520 I frames/sec is 260 transmitted and 260 received I frames/sec.
4. The frame length shown is an average value, and is defined as all bytes between the opening flag and the first CRC byte.
5. The results shown are preliminary.