AN13474

USB2.0 Certification Pre-test for i.MXRT Series

Rev. 0 — 14 January 2022 Application Note

Contents

1 Introduction

This application note describes how to perform the USB2.0 compliance pre-test for the i.MXRT series MCUs.

This document describes the test items, equipment, and tools used in the test and procedures of the USB2.0 compliance pre-test in detail.

2 Preparing for the test

2.1 Test boards

The boards listed below are certificated and registered in the USB-IF:

- MIMXRT1170-EVK
- MIMXRT1060-EVK
- IMXRT1050-EVKB
- MIMXRT1020-EVK
- MIMXRT1010-EVK
- MIMXRT685-EVK
- MIMXRT595-EVK

2.2 Test equipment and tools

Table 1 and Table 2 list the test equipment and the tests for which they are required. Keysight USB electrical test equipment was used in the testing, but you may use equipment from other vendors instead, such as, Tektronix and Lecroy.

Table 1. Digital oscilloscope and software

Test equipment			Tests		
Part number	Description	Manufacturer	Embedded host hi-speed	Device hi-speed	Low/Full-speed
DSOS604A	Digital real-time oscilloscope	Keysight (Agilent)	1	1	1
D9010USBC	USB 2.0 Compliance Test Software	Keysight (Agilent)	1	1	1
1131B	Differential probe amplifier	Keysight (Agilent)	1	1	N/A

Table continues on the next page...

Table 1. Digital oscilloscope and software (continued)

Test equipment			Tests		
Part number	Description	Manufacturer	Embedded host hi-speed	Device hi-speed	Low/Full-speed
E2678B	Differential Probe Head	Keysight (Agilent)	1	1	N/A
N2873A	Single-ended probe	Keysight (Agilent)	2	2	3
81160A	Pulse generator	Keysight (Agilent)	N/A	1	N/A
N2774A	Current probe	Keysight (Agilent)	N/A	N/A	1

Table 2. Test fixtures and accessories

Test equipment			Tests		
Part number	Description	Manufacturer	Embedded host hi-speed	Device hi-speed	Low/Full-speed
E2649-66401	Device hi-speed signal quality test fixture	Keysight (Agilent)	N/A	1	N/A
E2649-66402	Host high speed signal quality test fixture	Keysight (Agilent)	1	N/A	N/A
E2649-66403	Receiver sensitivity test fixture	Keysight (Agilent)	N/A	1	N/A
E2649-66405	Droop/Drop test fixture	Keysight (Agilent)	N/A	N/A	1
E2646B	USB inrush (SQiDD) test fixture	Keysight (Agilent)	N/A	N/A	1
82357B	USB/GPIB interface	Keysight (Agilent)	N/A	1	N/A
8493C	6 dB attenuators	Keysight (Agilent)	N/A	1	N/A
8120-4948 or equivalent	50-ohm-coaxial cable with male SMA connectors at both ends	Keysight (Agilent)	N/A	2	N/A

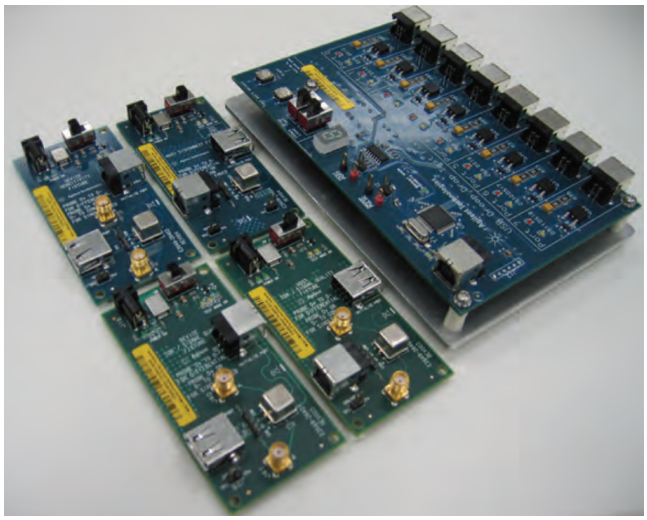

Figure 1. E2649 series hi-speed test fixtures

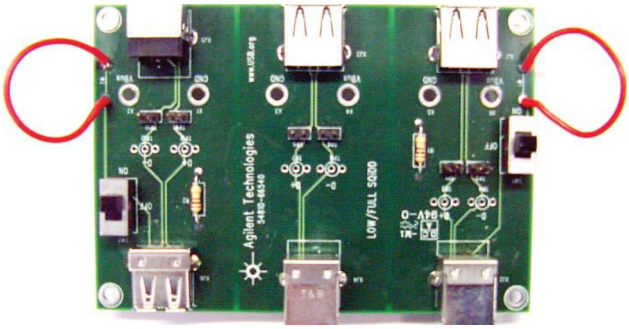

Figure 2. E2646B SOiDD test fixture

Figure 3. 1131B differential probe with E2678B head

2.3 Test demo

- For device test, `usb_device_hid_mouse_bm`, enable the macro `USB_DEVICE_CONFIG_COMPLIANCE_TEST` on `usb_device_config.h`.
- For embedded host test, `usb_host_msd_fatfs_bm`, enable the macro `USB_HOST_CONFIG_COMPLIANCE_TEST` on `usb_host_config.h`.

Only these two demos implement the whole USB certification function support. To run the whole compliance test, use these two demos.

3 Test procedures

3.1 Electrical test items and procedure

The USB automatic test software on the oscilloscope is needed for electrical test, and USBET is selected for automatic test, as shown in Figure 4. To open this software from the main menu of Infiniium oscilloscope, choose **Analyze > Automated Test Apps > D9010USBC USB Test App**.

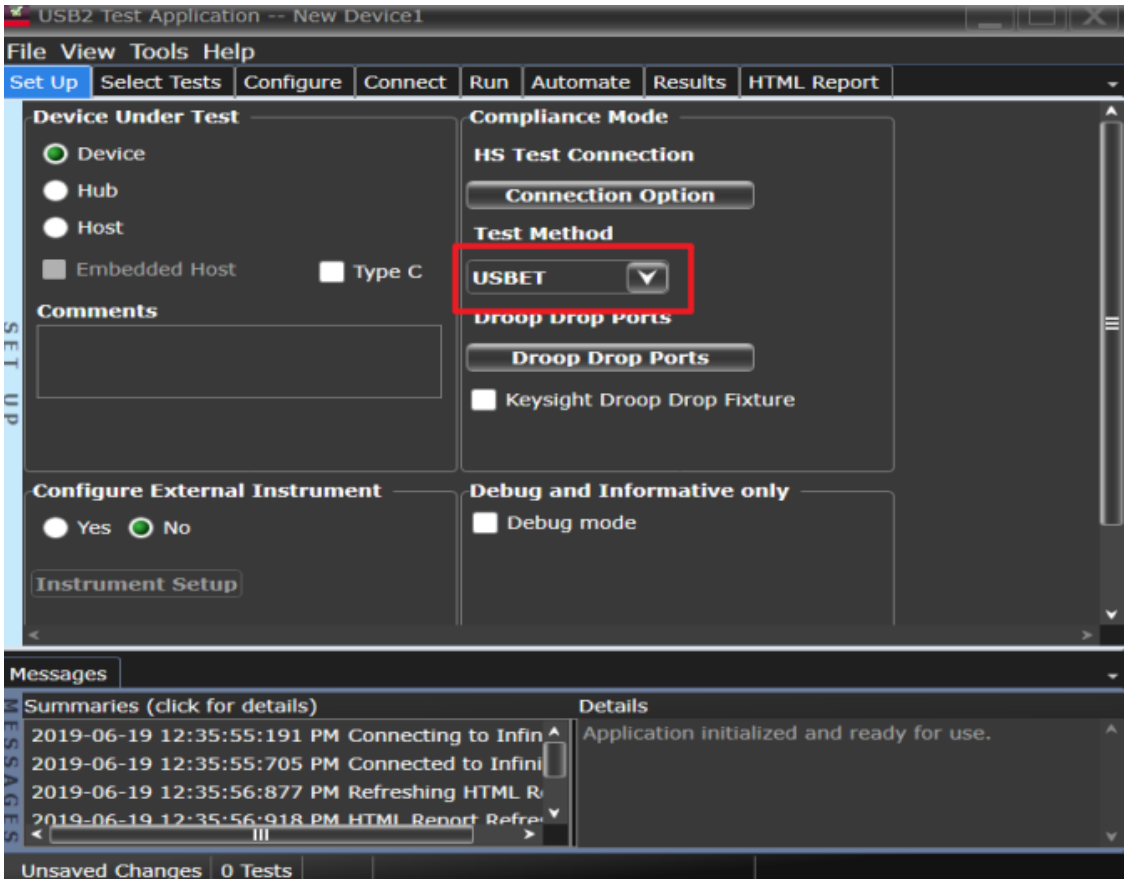

Figure 4. Initialization interface of test software

3.1.1 Device High-Speed signal test

To run a Device High-Speed signal test, perform the following steps:

1. Download and install the HS Electrical test tool on the test PC.
2. Send the test commands, and the device under test enters a specific test mode.

HSETT can be downloaded from https://www.usb.org/documents?search=HSET&items_per_page=50.

Device High-Speed signal test includes:

- Device High-Speed Signal Quality Test
- Device Packet Parameters test
- Device CHIRP Timing test
- Device Suspend/Reset/Resume Timing test
- Device Test J/K, SE0_NAK test
- Device Receiver Sensitivity test

Table 3 lists the electrical test limits for the High-Speed device.

Table 3. High-Speed device electrical test limits

Test name	Pass limits
EL_2 Data Rate	Within 480 Mb/s +/-0.05%
EL_4 Eye Pattern (without captive cable)	Must meet template 1 transform waveform requirements at TP3 (see Figure 5)
EL_6 Device Rise/Fall Time	> 500 ps
EL_7 Device Non-Monotonic Edge Test	Must have monotonic data transitions over the vertical openings
EL_21 Device Sync Field Length Test	32 bits, 65.62 ns <= VALUE <= 67.700 ns
EL_25 Device EOP Length Test	8 bits, 15.600 ns <= VALUE <= 17.700 ns
EL_22 Measure Interpacket Gap Between Second and Third Packets	16.640 ns <= VALUE <= 399.400 ns
EL_22 Measure Interpacket Gap Between First and Second Packets	16.640 ns <= VALUE <= 399.400 ns
EL_28 Measure Device CHIRP-K Latency	2.500 µs <= VALUE <= 6.000000 ms
EL_29 Measure Device CHIRP-K Duration	1.000 ms <= VALUE <= 7.000 ms
EL_31 Device High-Speed Terminations Enable and D+ Disconnect Time	1 ns <= VALUE <= 500.000 µs
EL_40 Device Resume Timing Response	Must transition back to high-speed operation within two-bit times from the end of resume time signaling
EL_27 Device CHIRP Response to Reset from High-Speed Operation	3.100 ms <= VALUE <= 6.000 ms
EL_28 Device CHIRP Response to Reset from Suspend	2.500 µs <= VALUE <= 6.000000 ms
EL_38 EL_39 Device Suspend Timing Response	3.000 ms <= VALUE <= 3.125 ms
EL_8 Device J Test	360 mV <= D+ <= 440 mV -10 mV <= D- <= 10 mV
EL_8 Device K Test	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
EL_9 Device SE0_NAK Test	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV
EL_18 Minimum SYNC Field	Detect the end of the SYNC field within 12-bit times
EL_17 Receiver sensitivity	VALUE <= +/- 200 mV
EL_16 Squelch	VALUE >= +/- 100 mV

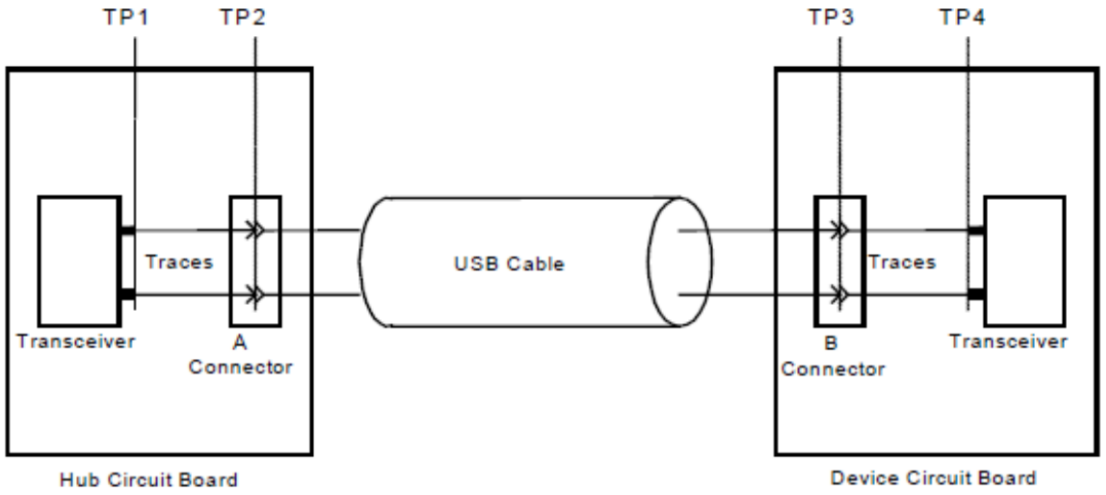

Figure 5. HS signal measurement planes

According to the USB2.0 Specification, if the DUT does not contain a captive cable, it must meet the requirement of the Template 1 for the eye patterns. Transmit eye patterns specify the minimum and maximum limits, as well as limits on timing jitter, within which a driver must drive signals at each of the specified test planes. Figure 6 shows Template 1.

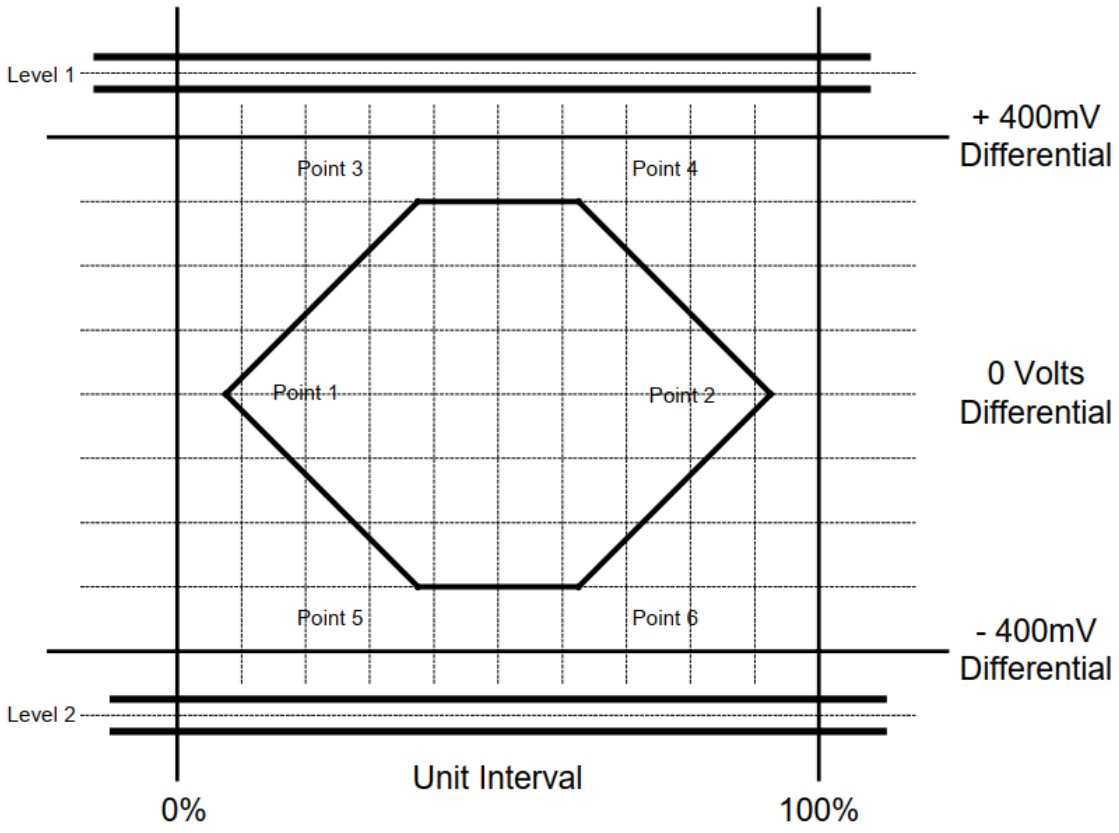

Figure 6. Template 1 for device without a captive cable

3.1.1.1 Device Hi-speed Signal Quality Test procedure

This test measure the transmitter's ability to carry out effective hi-speed transmission. For the device, measure the hi-speed signal quality on the upstream port. Table 4 lists the equipment used in the test.

Table 4. Equipment used in Device Hi-Speed Signal Quality Test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Differential probe	Keysight 1131B with E2678B	1
Host test bed computer	Any computer with hi-speed USB ports	1
Device HS Signal Quality test fixture and 4" USB cable	Keysight E2649-66401	1
5 V power supply	Keysight 0950-2546 or equivalent	1

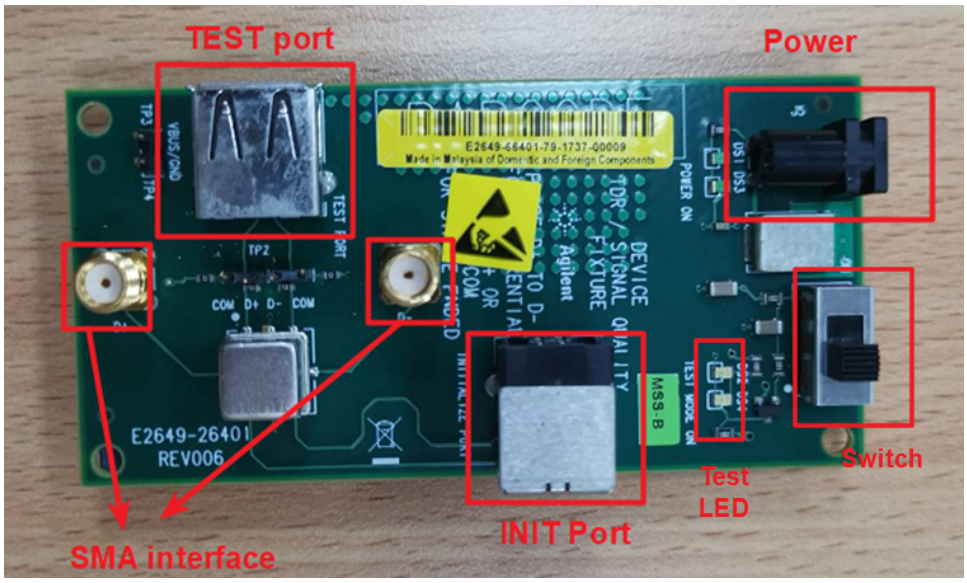

Figure 7. E2649-66401 entity

For the test, perform the following steps:

1. Open the test software in on the oscilloscope, select **Device** as the DUT, check the test items shown in Figure 8, and set the test type to **Hi-Speed Near End** in the **Configure** tab.

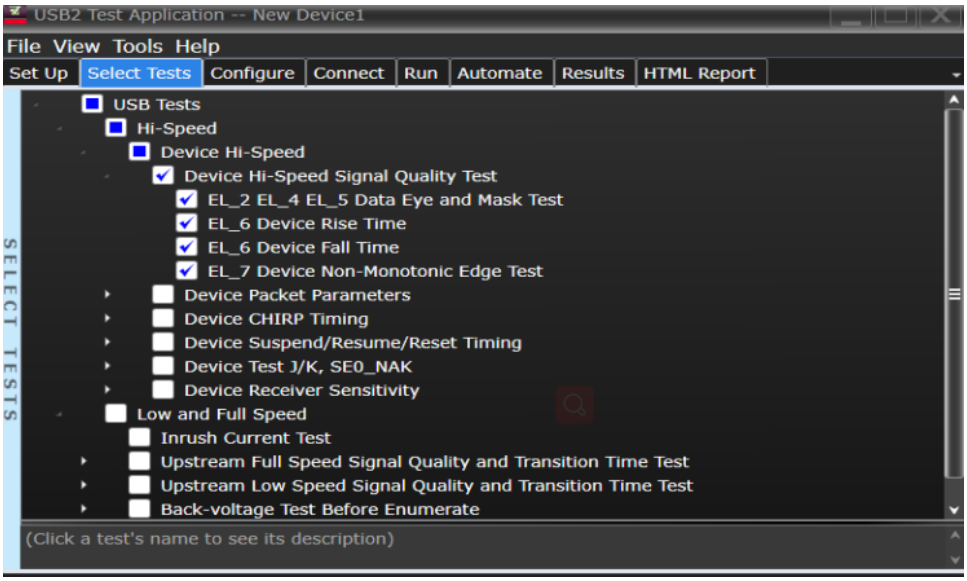

Figure 8. Device Hi-Speed Signal Quality Test

2. Connect the 50 ohm terminator to the SMA interface on the fixture, as shown in Figure 9.

Figure 9. 50 ohm SMA terminator

3. Connect the test equipment, fixture, and oscilloscope, as shown in Figure 10.

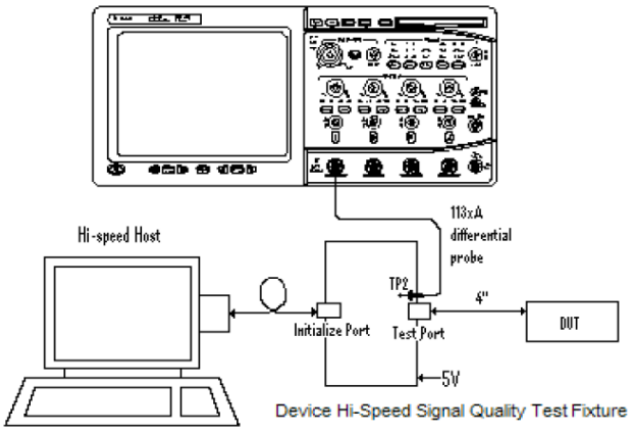

Figure 10. Device Hi-Speed Signal Quality test connection

4. Attach the 5 V power supply to **J5** of the E2649-66401 Device Hi-Speed signal quality test fixture. Leave the **TEST** switch at the **OFF** position. Verify that the green Power LED is lit and the yellow Test LED is not lit.

5. Use a 4" USB cable to connect the **[TEST PORT]** of the Device Hi-speed Signal Quality test fixture into the upstream facing port of the device under test.
6. Use a 5-meter USB cable to connect the **[INIT PORT]** of the test fixture to a Hi-speed capable port of the Test Bed Computer.

Figure 11. Device connection physical map

7. Power on the device and click the **Run Tests** button of the Automated Test software on the oscilloscope. As shown in Figure 12, invoke the HS Electrical Test Tool software on the Hi-Speed Electrical Test Bed computer, according to the type of PC's USB Controller. It is divided into EHCI HSETT and XHCI HSETT. Both can be downloaded from the USB-IF website. Select Device and click the **TEST** button to enter the **Device Test** menu. The DUT is enumerated with VID of the device shown together with the root port in which it is connected. For i.MX RT boards as DUT, the default VID is `0x1fc9` and PID is `0x0091`.

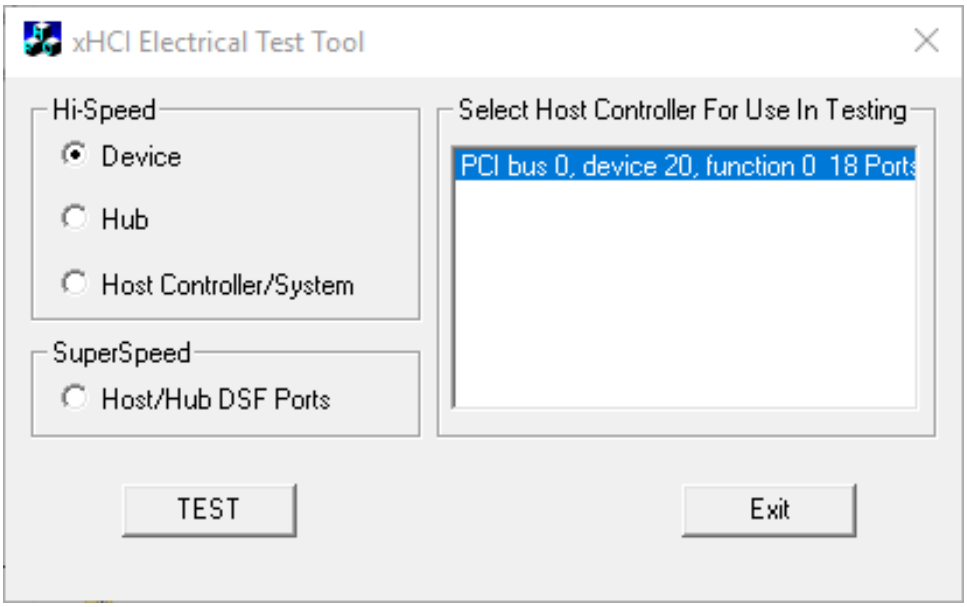

Figure 12. HSETT main interface

8. Select **TEST_PACKET** from the **Device Command** drop-down menu, as shown in Figure 13. Click **EXECUTE**. The device under test continuously transmits test packets.

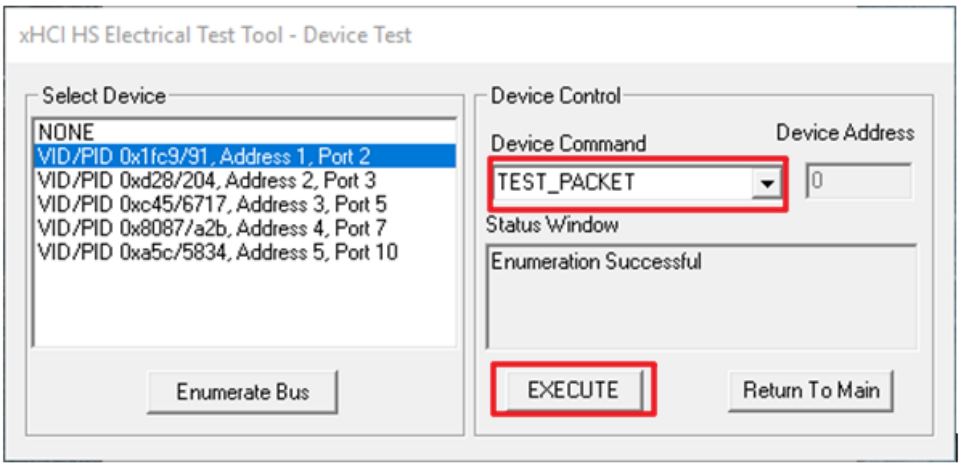

Figure 13. HSETT test packet command

9. Place the Test Switch (S1) in the **TEST** position according to the prompt on the oscilloscope. Verify that the yellow TEST LED is lit. The waveform that the oscilloscope catches must be similar to the waveform prompted in the Automated Test software.

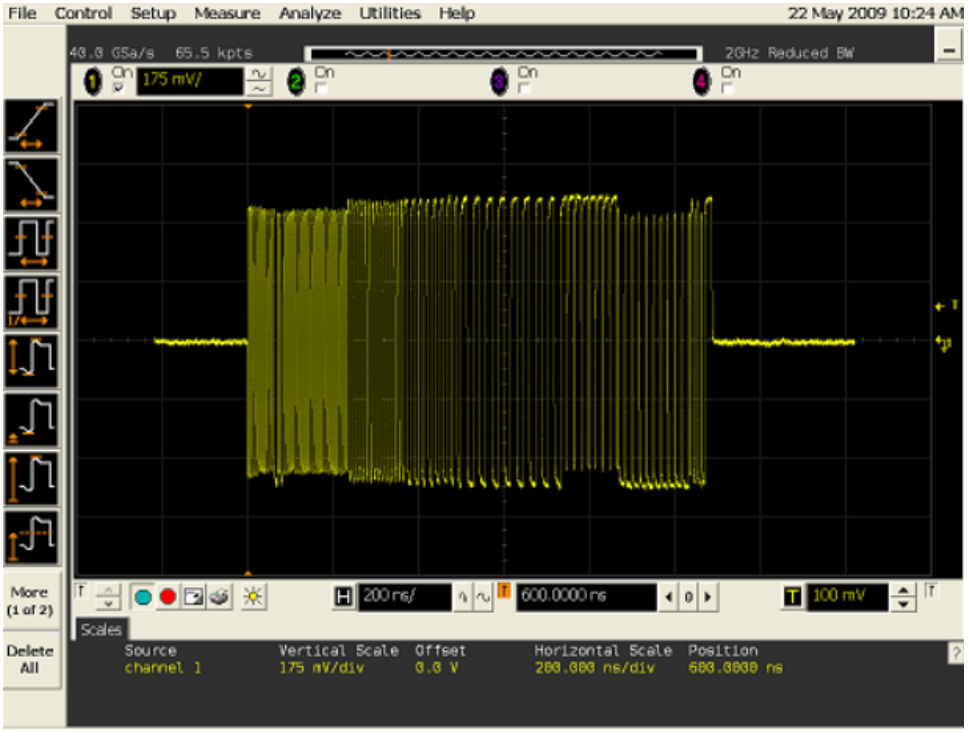

Figure 14. Prompted device test packet waveform

10. When the **Testing Complete** dialog appears, click **OK**. The **Results** tab shows the test results.

Pass	# Failed	# Trials	Test Name	Actual Value	Margin	Pass Limits
✓	0	1	EL_2 EL_4 EL_5 Data Eye and Mask Test	Pass	100.0 %	Pass/Fail
ⓘ		1	EL_6 Device Rise Time	769.220 ps		Information Only
ⓘ		1	EL_6 Device Fall Time	718.730 ps		Information Only
✓	0	1	EL_7 Device Non-Monotonic Edge Test	Pass	100.0 %	Pass/Fail

Figure 15. Device Hi-Speed Signal Quality Test result

3.1.1.2 Device Packet Parameters test procedure

This test is used to check whether the length of each field in the USB message and the interval between messages is accurate. The equipment used in the test is same as device high-speed signal quality test, except that the 5 V power cable can be unplugged.

To run the test, perform the following steps:

1. Select the test items as shown in Figure 16, connect the test equipment as shown in Figure 10, and connect the 50 ohm terminator to the SMA interface on the fixture.

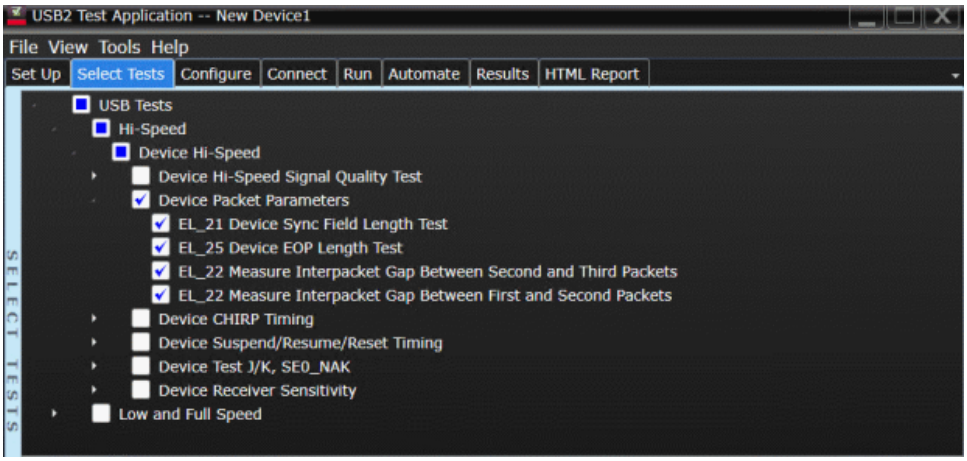

Figure 16. Device packet parameters test

2. The connection of the DUT, PC, and oscilloscope probe is the same as the signal quality test.
3. To restore the device to normal operation, cycle the device power and click **Run Tests** on the oscilloscope. As shown in Figure 17, in the **Device Test** menu of the HS electrical tool, click **Enumerate Bus** once. Observe the oscilloscope and verify the SOFs packets are being transmitted on the port under test.

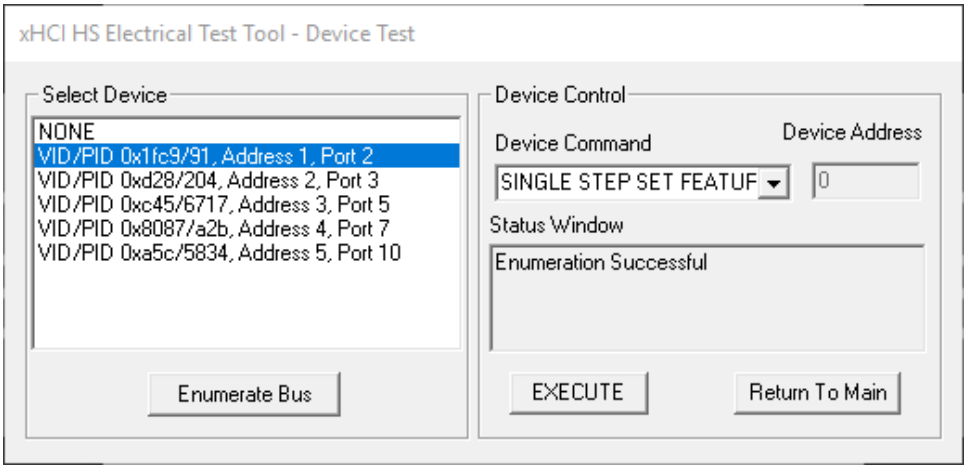

Figure 17. HSETT single step set feature command

4. According to the prompt of the oscilloscope, select **SINGLE STEP SET FEATURE** from the **Device Command** window. Click **EXECUTE** once. Verify that the waveform the oscilloscope catch is similar to the waveform prompted in the Automated Test software. Then click **OK** to the next step.

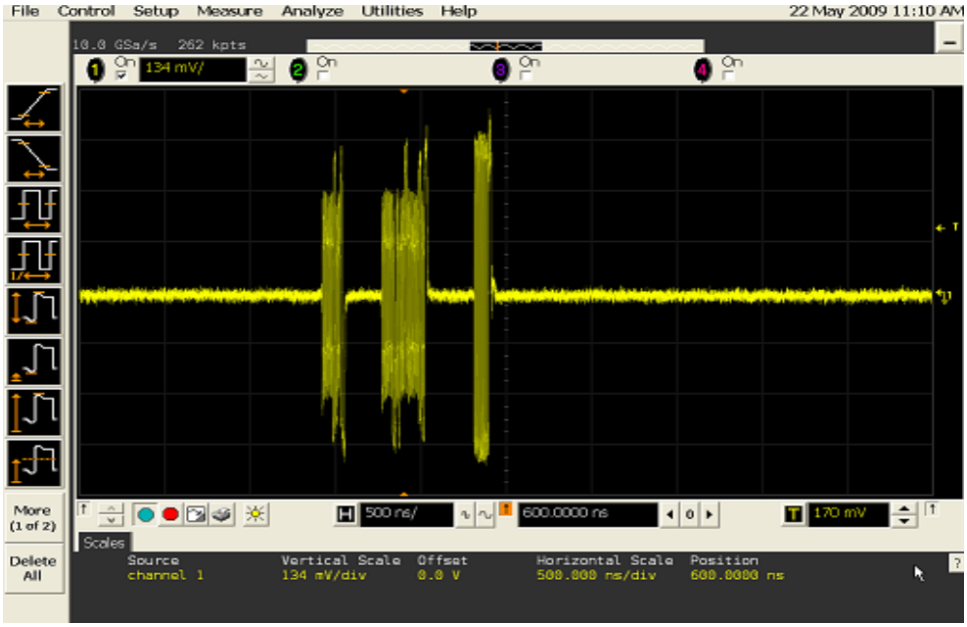

Figure 18. Prompted waveform

5. In the **Device Test** menu of the HS electrical test tool, click **Step** once again. This is the second step of the two-step Single Step Set Feature command. Verify that the waveform the oscilloscope catch is similar to the waveform prompted in the automated test software. When the **Testing Complete** dialog appears, click **OK**.

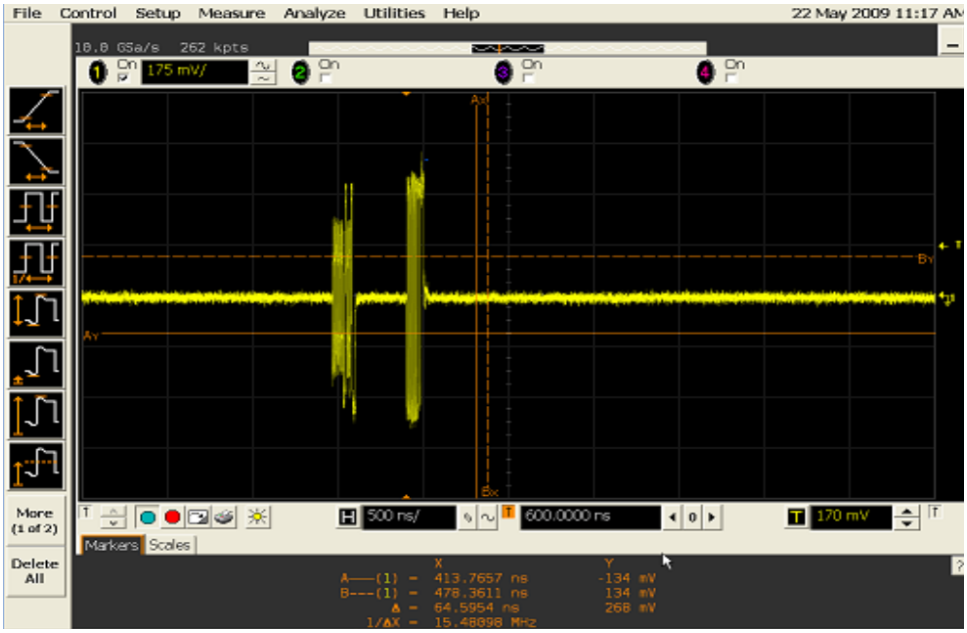

Figure 19. Prompted waveform

3.1.1.3 Device CHIRP Timing test procedure

This item tests the ChirpJ and ChirpK signals generated during the high-speed handshake procedure. Table 5 lists the equipment used in the test.

Table 5. Equipment used in Device CHIRP Timing test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Single-ended probe	Keysight N2873A	2
Host test bed computer	Any computer with hi-speed USB ports	1
Device HS Signal Quality test fixture and 4” USB cable	Keysight E2649-66401	1
5 meter USB 2.0 hi-speed cable	Any listed on USB-IF website	1

To run the test, perform the following steps:

1. Select the test items in the automated test software on the oscilloscope, as shown in Figure 20.

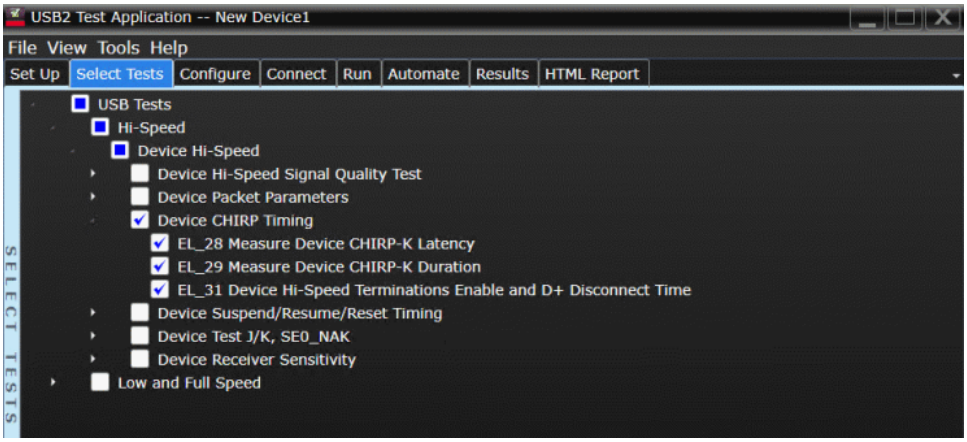

Figure 20. Device CHIRP Timing test

2. Connect the test equipment as shown in Figure 21. According to the prompt of the test software, attach the single-end probes on Channel 2 to D- of TP2 and Channel 3 to D+ of TP2. Connect the 50 ohm terminator to the SMA interface on the fixture.

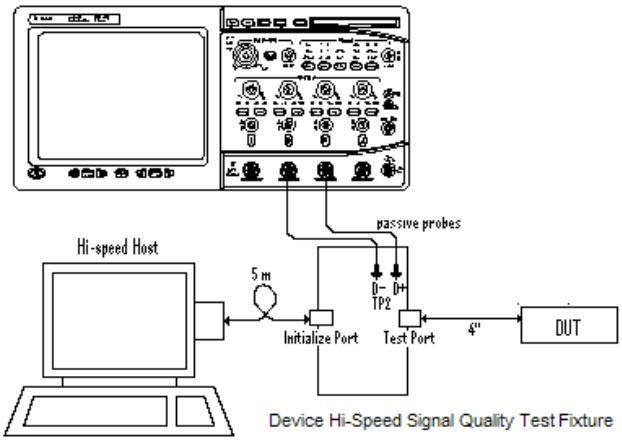

Figure 21. Device CHIRP Timing Test connection

3. To restore the device to normal operation, cycle the device power and click **Run Tests** on the oscilloscope. On the HS electrical test tool software, click **Enumerate Bus** once, and the oscilloscope captures and measures the Chirp handshake.
4. When the **Testing Complete dialog** appears, click **OK**.

3.1.1.4 Device Suspend/Reset/Resume Timing test procedure

This test measures the timing of the device's response to the suspend, resume, and reset signals from the host. The equipment used in the test is same as device CHIRP Timing test.

To run the test, perform the following steps:

1. Select the test items in the Automated Test software on the oscilloscope as shown in .

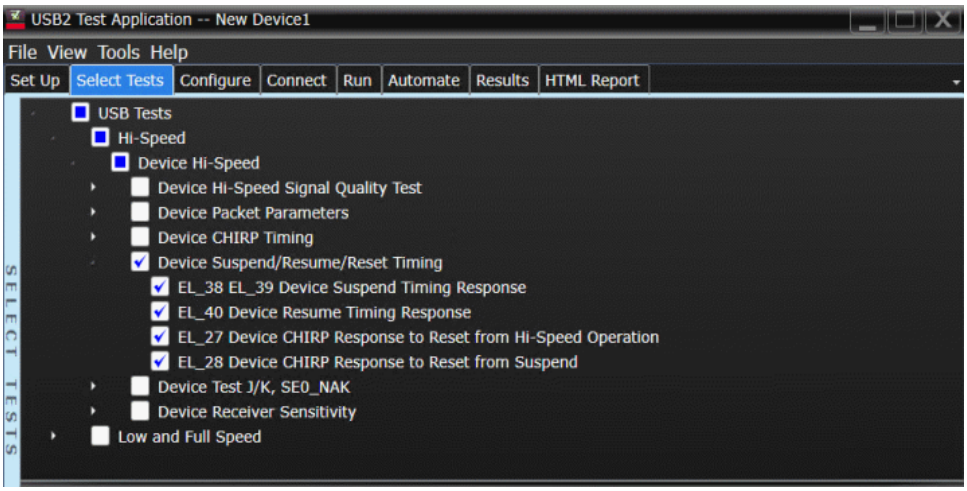

Figure 22. Device Suspend/Reset/Resume Timing Test

2. The connection of the DUT, PC, and oscilloscope probes is the same as the Device CHIRP Timing test.
3. Reset the power for the EVK and click **Run Tests** on the oscilloscope. On the **Device Test** menu of the HS electrical test tool software, click **Enumerate Bus** once.

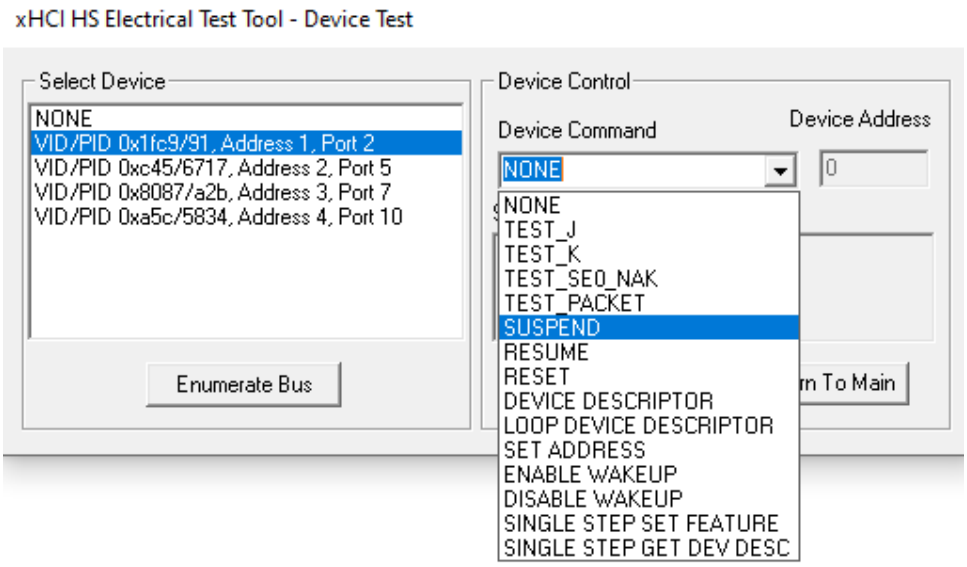

Figure 23. HSETT suspend, resume, and reset commands

4. As shown in Figure 23, select the DUT and **SUSPEND** from the **Device Command** drop-down menu. Click **EXECUTE** once to place the device into suspend. The waveform that the oscilloscope catches is similar to the waveform prompted in the automated test software. Click **OK**.

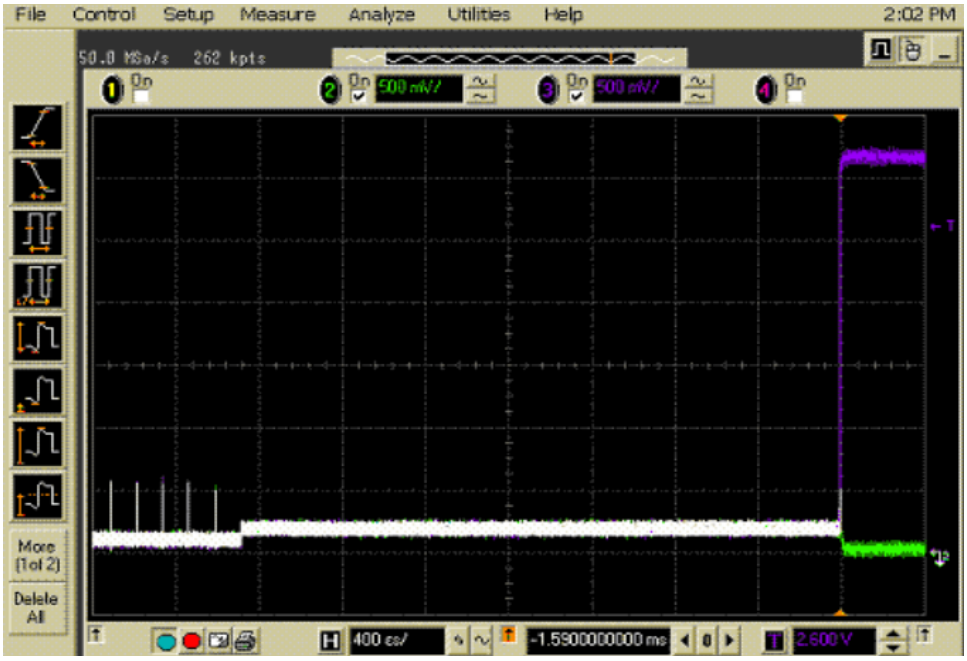

Figure 24. Prompted device suspend waveform

5. On the **Device Test** menu of the HS electrical test tool, select **RESUME** from the **Device Command** drop-down menu. Click **EXECUTE** once to resume the device from suspend. The waveform that the oscilloscope catches is similar to the waveform prompted in the automated test software. Click **OK**.

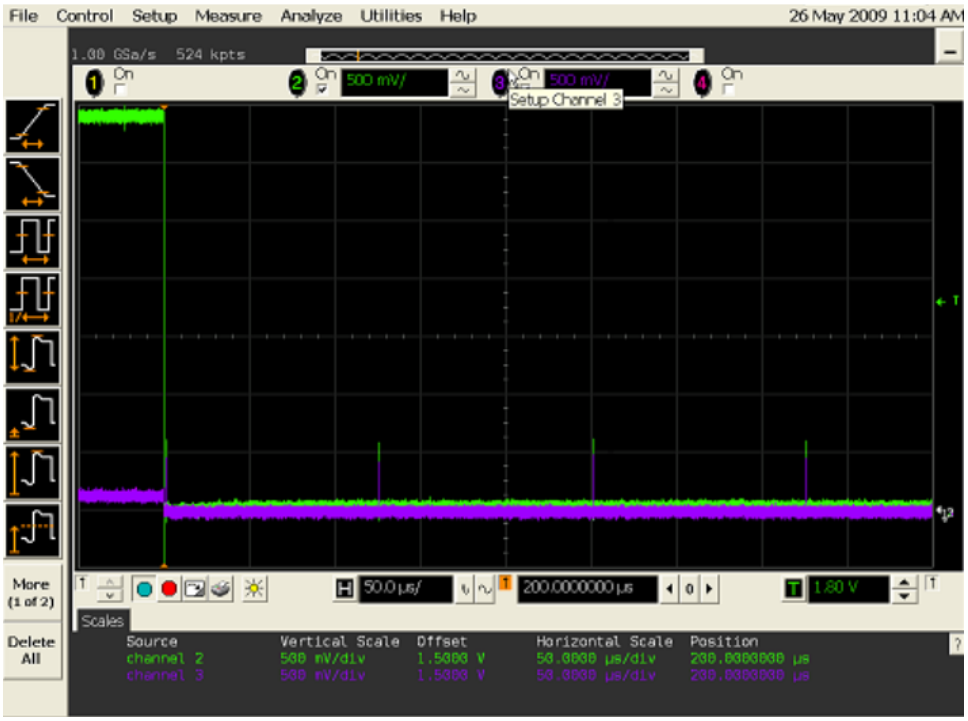

Figure 25. Prompted device resume waveform

6. On the **Device Test** menu of the HS electrical test tool, select **RESET** from the **Device Command** drop-down menu. Click **EXECUTE** once to reset the device operating in high speed. The waveform that the oscilloscope catches is similar to the waveform prompted in the automated test software. Click **OK**.

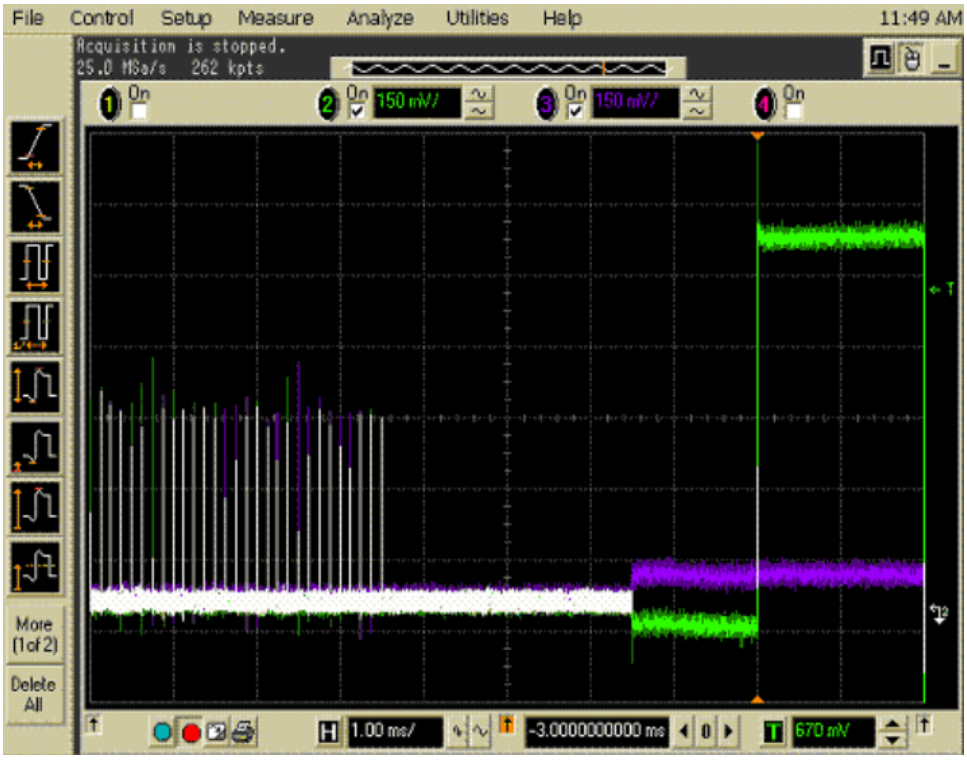

Figure 26. Prompted device reset from hi-speed waveform

7. Select **SUSPEND** and click **EXECUTE** again to place the device into suspend once more. To reset the device from suspend, select **RESET** and click **EXECUTE** once. The waveform that the oscilloscope catches is similar to the waveform prompted in the automated test software. When the **Testing Complete** dialog appears, click **OK**.

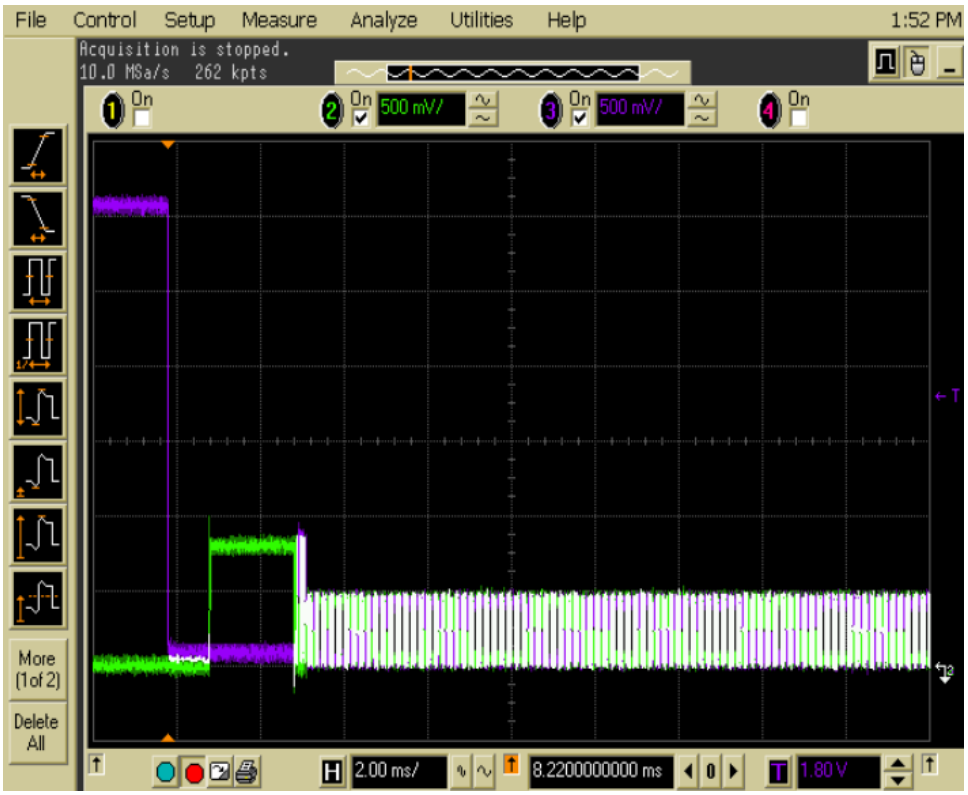

Figure 27. Prompted device reset from suspend waveform

3.1.1.5 Device Test J/K, SE0_NAK test procedure

This item tests the voltage of the two data lines when the device is in the three differential signal states of J, K, and SE0. Table 6 lists the equipment used in the test.

Table 6. Equipment used in Device Test J/K, SE0_NAK test

Item	Model	Quantity
Multimeter	Any	1
Host test bed computer	Any computer with hi-speed USB ports	1
Device HS Signal Quality test fixture and 4''USB cable	Keysight E2649-66401	1
5 V power supply	Keysight 0950-2546 or equivalent	1
5 meter USB 2.0 hi-speed cable	Any listed on USB-IF website	1

To run the test, perform the following steps:

1. Select the test items in the automated test software on the oscilloscope, as shown in Figure 28. There is no need to use an oscilloscope to capture the waveform in this test. To form a complete report, use a multimeter to measure the voltage and input the measurement into the test software.

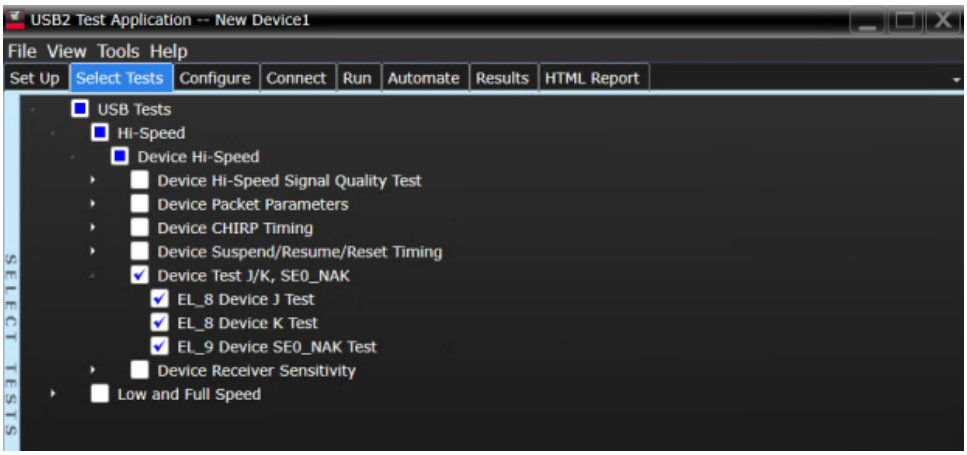

Figure 28. Device Test J/K, SE0_NAK test

2. As shown in Figure 29, connect the test equipment and place the switch in the test switch to **OFF** position. Verify that the green power LED is lit and the yellow test LED is OFF.

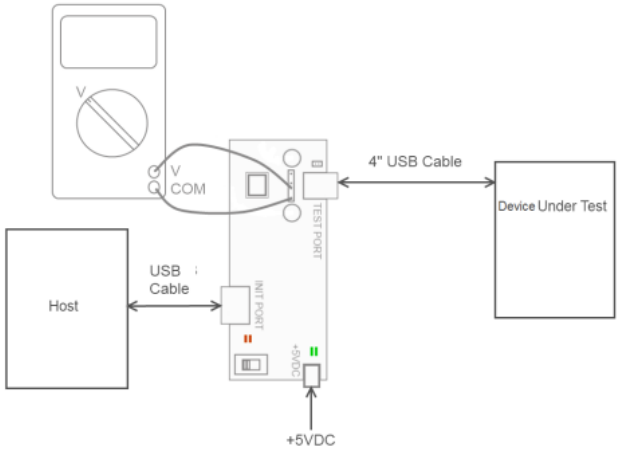

Figure 29. Device Test J/K, SE0_NAK test connection

3. Reset the power for the EVK and click **Run Tests** on the oscilloscope. On the **Device Test** menu of the HS electrical test tool, click **Enumerate Bus** once.
4. Select **TEST_J** from the **Device Command** drop-down menu, as shown in Figure 30. To place the device into `TEST_J` test mode, click **EXECUTE** once.

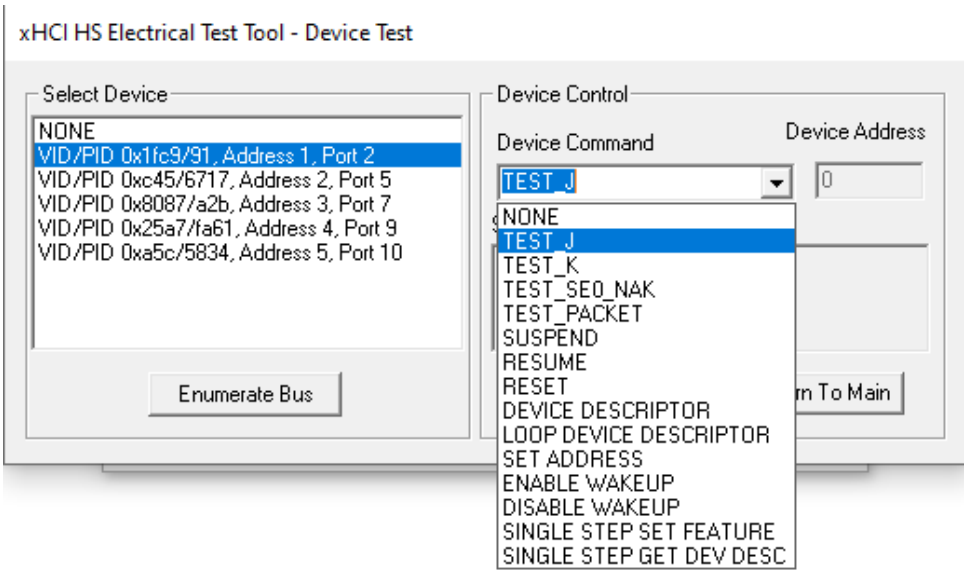

Figure 30. HSETT TEST_J. TEST_K and Test_SE0_NAK command

5. Switch the test fixture into the **TEST** position. Use a multimeter to measure the DC voltage on the D+/D- lines at TP2 with respect to GND. Record the measurement in the pop-up dialog of the oscilloscope. Click **OK**.

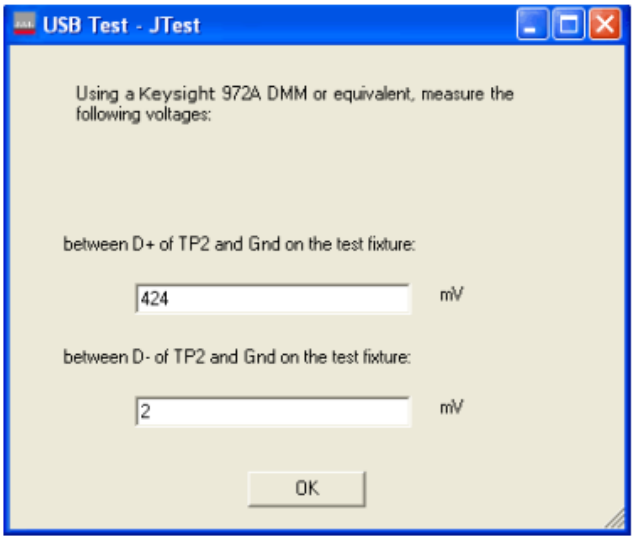

Figure 31. TEST_J dialog

6. Return the test switch of the test fixture to the **NORMAL** position. Reset the power for the EVK. On the **Device Test** menu of the HS electrical test tool, click **Enumerate Bus** once.
7. Select **TEST_K** from the **Device Command** drop-down menu. To place the device into TEST_K test mode, click **EXECUTE** once.
8. Switch the test fixture into the **TEST** position and verify that the yellow test LED is lit. Use a multimeter to measure the DC voltage on the D+/D- lines at TP2 with respect to GND. Record the measurement in the pop-up dialog of the oscilloscope. Click **OK**.

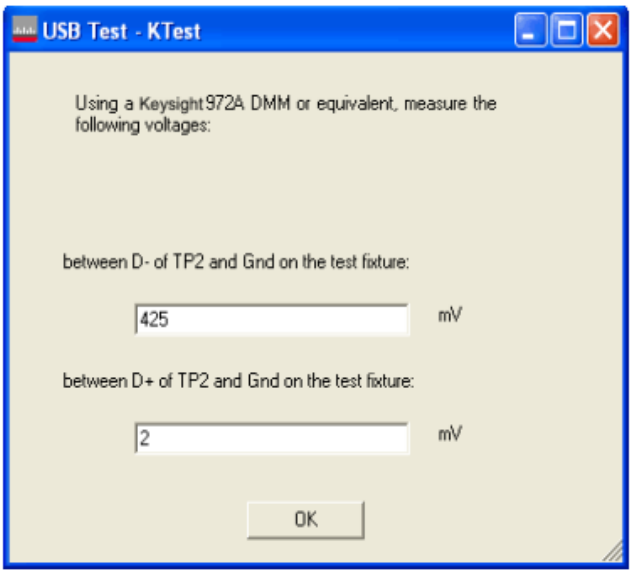

Figure 32. TEST_K dialog

9. Return the test switch of the test fixture to the **NORMAL** position. Reset the power for the EVK. On the **Device Test** menu of the HS electrical test tool, click **Enumerate Bus** once.
10. Select **TEST_SE0_NAK** from the **Device Command** drop-down menu. To place the device into TEST_SE0_NAK mode, click **EXECUTE** once.
11. Switch the test fixture into the **TEST** position. Verify that the yellow test LED is lit. Use a multimeter to measure the DC voltage on the D+/D- lines at TP2 with respect to GND. Record the measurement in the pop-up dialog of the oscilloscope. Click **OK**.

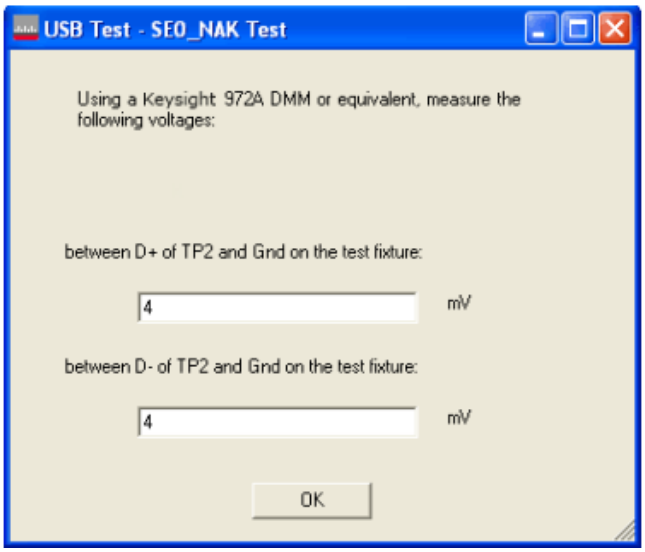

Figure 33. SE0_NAK dialog

3.1.1.6 Device Receiver Sensitivity test procedure

Due to the lack of signal generating equipment, this application note does not introduce the pre-test of the receiver sensitivity but lists the procedure of the receiver sensitivity test. Table 7 lists the equipment used in the test.

Table 7. Equipment used in Device Receiver Sensitivity test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Differential probe	Keysight 1131B with E2678B	1
Host test bed computer	Any computer with hi-speed USB port	1
Receiver Sensitivity test fixture and 4" USB cable	Keysight E2649-66403	1
5 V power supply	Keysight 0950-2546 or equivalent	1
Digital signal generator	Keysight 81160A	1
USB/GPIB interface	Keysight 82357B	1
6 dB attenuators	Keysight 8493C	2
50-ohm-coaxial cable with male SMA connectors at both ends	Keysight 8120-4948	2
5-meter USB2.0 hi-speed cable	Any listed on USB-IF website	1

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 34. Connect the equipment and test fixture, as shown in Figure 35. Verify that the green power LED is lit and the yellow test LED is OFF.

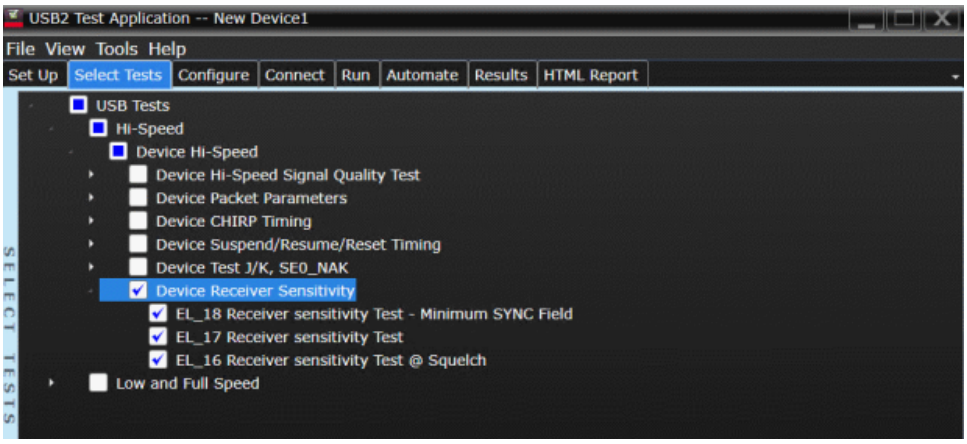

Figure 34. Device Receiver Sensitivity test

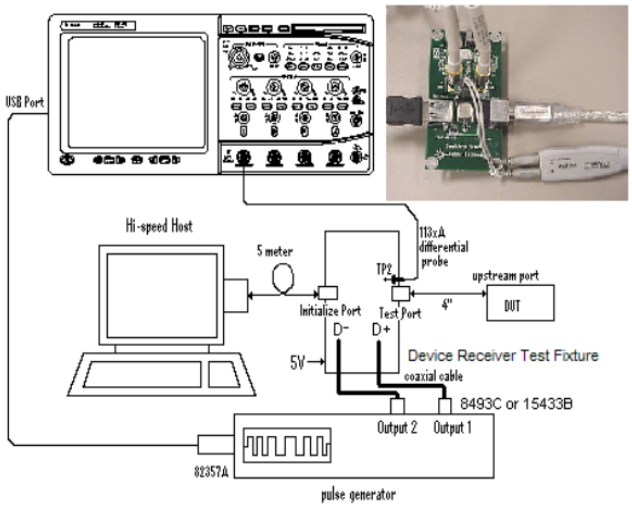

Figure 35. Device Receiver Sensitivity test connection

2. Connect the 81130A pulse generator to the oscilloscope through the 82357A USB/GPIB Interface. Connect the 8493C 6 dB attenuators to OUTPUT1 and OUTPUT2 of Agilent 81130A Pulse/Pattern Generator.
3. Use 8120-4948 SMA cables to connect OUTPUT1 to SMA1 (D+) of the E2649-66403 device receiver sensitivity test fixture. Use 8120-4948 SMA cables to connect OUTPUT2 to SMA2 (D-) of the E2649-66403 device receiver sensitivity test fixture.
4. Reset the power for the EVK and click **Run Tests** on the oscilloscope. On the **Device Test** menu of the HS electrical test tool, click **Enumerate Bus** once.
5. Select **TEST_SE0_NAK** from the **Device Command** drop-down menu. To place the device into TEST_SE0_NAK test mode, click **EXECUTE** once.
6. Place the test fixture Test Switch (S1) into the **TEST** position. This operation switches in the data generator in place of the host controller. The data generator emulates the **IN** packets from the host controller.
7. When the **Testing Complete** dialog appears, click **OK**.

3.1.2 Embedded Host Hi-Speed signal test

In a normal host test, the host is a product installed the HS electrical test tool based on windows system to run the test. But for the Embedded Host test, it cannot run the software. USB-IF defines a method of entering the specified test modes via PID/VID detection. The certification lab provides a PIDVID board to perform the host or embedded host test. To set this board to different PID, set the DIP switch, as shown in Figure 36.

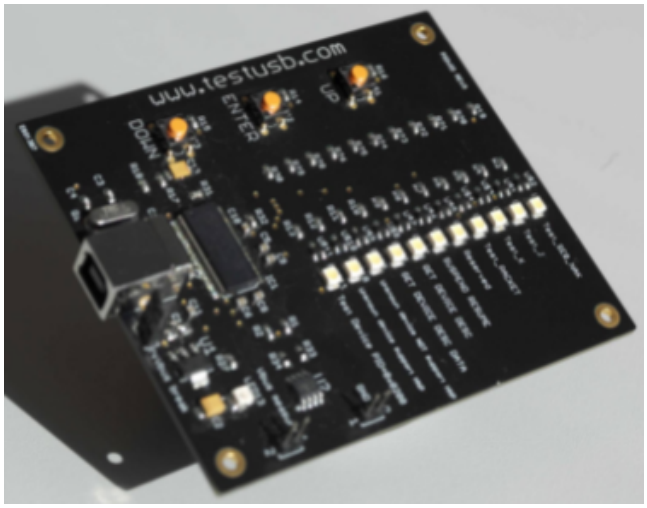

Figure 36. PIDVID board

Due to the lack of this test board, to achieve the same function, this application note uses another EVK board to download the program with different PID to the EVK. When performing the test, fix the VID of the EVK board as `0x1A0A`, modify the PID of the EVK, and connect the EVK to the host under test through the test fixture. The host enters the specified test mode. Table 8 lists the commands for different PID.

Table 8. Test modes PID definitions

PID	Test mode
0x0101	TEST_SE0_NAK
0x0102	TEST_J
0x0103	TEST_K
0x0104	TEST_PACKET
0x0105	RESERVED
0x0106	HS_HOST_PORT_SUSPEND_RESUME
0x0107	SINGLE_STEP_GET_DEV_DESC
0x0108	SINGLE_STEP_ GET_DEV_DESC_DATA

The embedded Host Hi-Speed signal test items include:

- Embedded Host Hi-Speed Signal Quality test
- Embedded Host Controller Packet Parameters test
- Host CHIRP Timing test
- Host Suspend/Resume Timing test
- Host Test J/K, SE0_NAK test

Table 9 describes the electrical test limits for the high-speed host.

Table 9. HS host electrical test limits

Test name	Pass limits
EL_2 Data rate	Within 480 Mb/s +/-0.05%
EL_3 Data Eye and Mask Test	Must meet Template 1 transform waveform requirements at TP2
EL_6 Host rise/fall time	>500 ps
EL_7 Host Non-Monotonic Edge Test	Must have monotonic data transitions over the vertical openings
EL_21 Sync Field Length Test	32 bits, 65.62 ns <= VALUE <= 67.700 ns
EL_25 EOP Length Test	8 bits, 15.620 ns <= VALUE <= 17.700 ns
EL_23 Inter-packet gap between first 2 Packets Test	183.000 ns <= VALUE <= 399.400 ns
EL_55 SOF EOP Width Test	40 bits, 81.100 ns <= VALUE <= 83.388 ns
EL_22 Inter-packet gap between Host and Device Packet Test	16.640 ns <= VALUE <= 399.90 ns
EL_33 CHIRP timing response	1 ns <= VALUE <= 100.000 µs
EL_34 CHIRP J/K width	40.000 µs <= VALUE <= 60.000 µs
EL_35 SOF Timing Response	100.000 µs <= VALUE <= 500.000 µs
EL_39 Suspend Timing Response	3.000 ms <= VALUE <= 3.125 ms
EL_41 Resume Timing Response	VALUE <= 3.000 ms
EL_8 Host J Test	360 mV <= D+ <= 440 mV -10mV <= D- <= 10 mV
EL_8 Host K Test	360 mV <= D- <= 440 mV -10 mV <= D+ <= 10 mV
EL_9 Host SE0_NAK Test	-10 mV <= D+ <= 10 mV -10 mV <= D- <= 10 mV

Select the Host option and check **Embedded Host** in the USB automated test software on the oscilloscope, as shown in Figure 37.

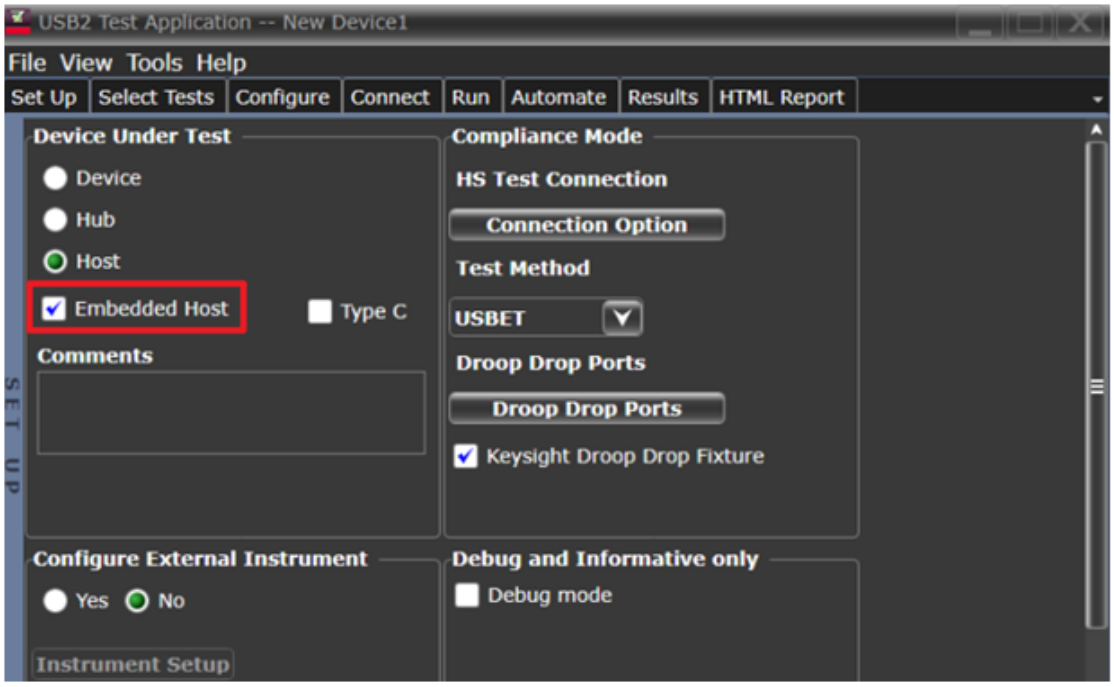

Figure 37. Embedded Host Test

3.1.2.1 Host Hi-Speed Signal Quality test procedure

Table 10 lists the equipment used in the test.

Table 10. Equipment used in Device Hi-Speed Signal Quality test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Differential probe	Keysight 1131B with E2678B	1
PIDVID board	MIMXRT1010-EVK simulated	1
Host Hi-Speed Signal Quality test fixture and 4" USB cable	Keysight E2649-66402	1
5 V power supply	Keysight 0950-2546 or equivalent	1
USB cable	Micro-B plug OTG cable	1

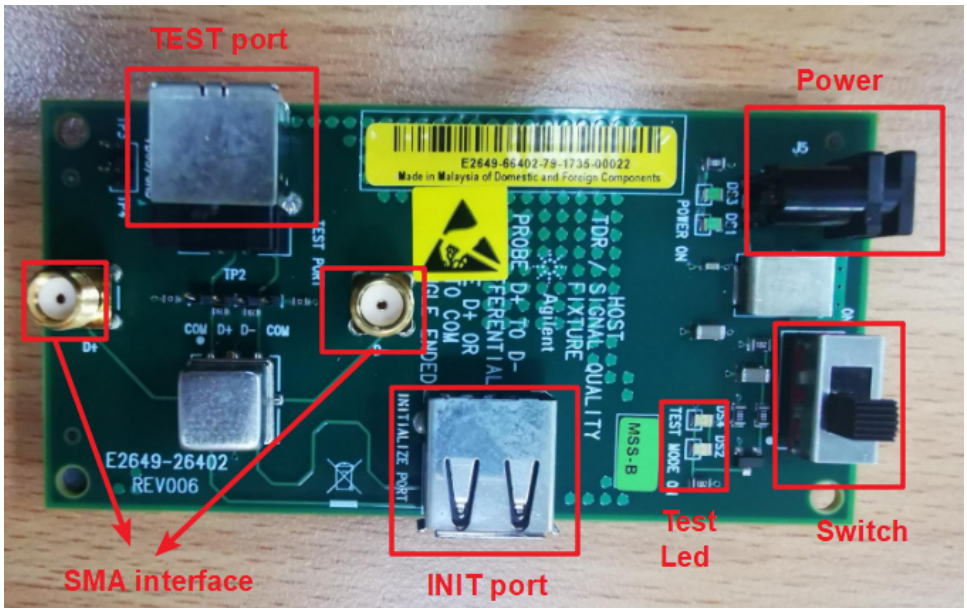

Figure 38. E2649-66402 entity

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 39. Before running the test, set the test type to **Hi-Speed Near End**.

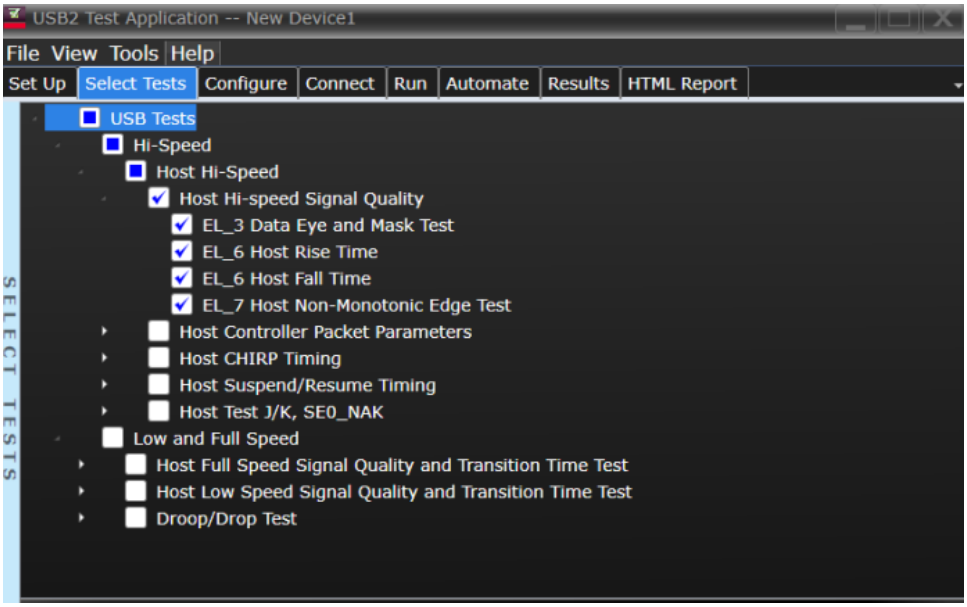

Figure 39. Device Hi-Speed Signal Quality test

2. Connect the test-embedded host board, fixture, and oscilloscope, as shown in Figure 40. Connect the 50 ohm terminator to the SMA interface on the fixture.

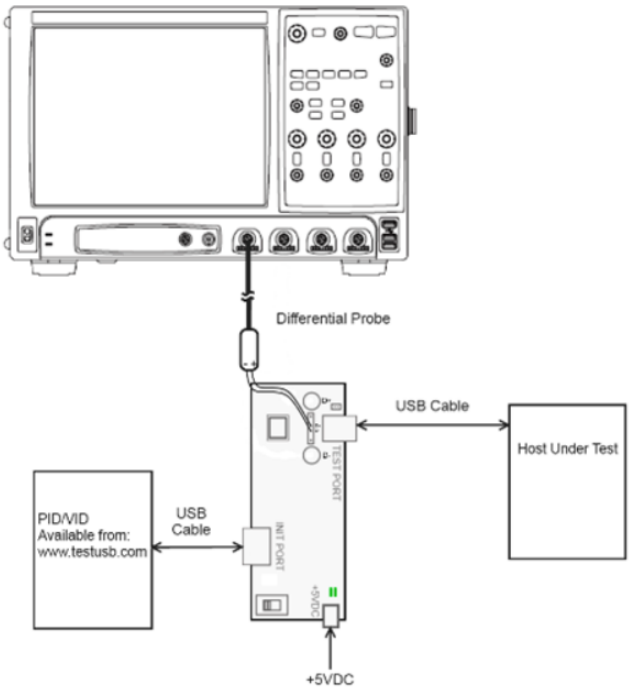

Figure 40. Device Hi-Speed Signal Quality test connection

3. Attach the 5 V power supply to J5 of the E2649-26402 Hi-Speed Signal Quality test fixture. Verify that the green power LED, **D1**, is lit.
4. Use an OTG cable to connect the Micro-AB receptacles. Use a 4-inch USB cable to connect the **Test Port** of the test fixture into the downstream facing port of the type-A connector of the OTG cable.
5. Choose a USB device demo. Modify the VID to `0x1A0A` and PID to `0x0104`. Compile and download it to a MIMXRT1010-EVK. Connect the USB port of MIMXRT1010-EVK to the initialize port of the fixture.
6. Attach the differential probe on channel 1 to D+/D- of TP2 on the test fixture. Ensure that the + polarity on the probe lines up with D+.

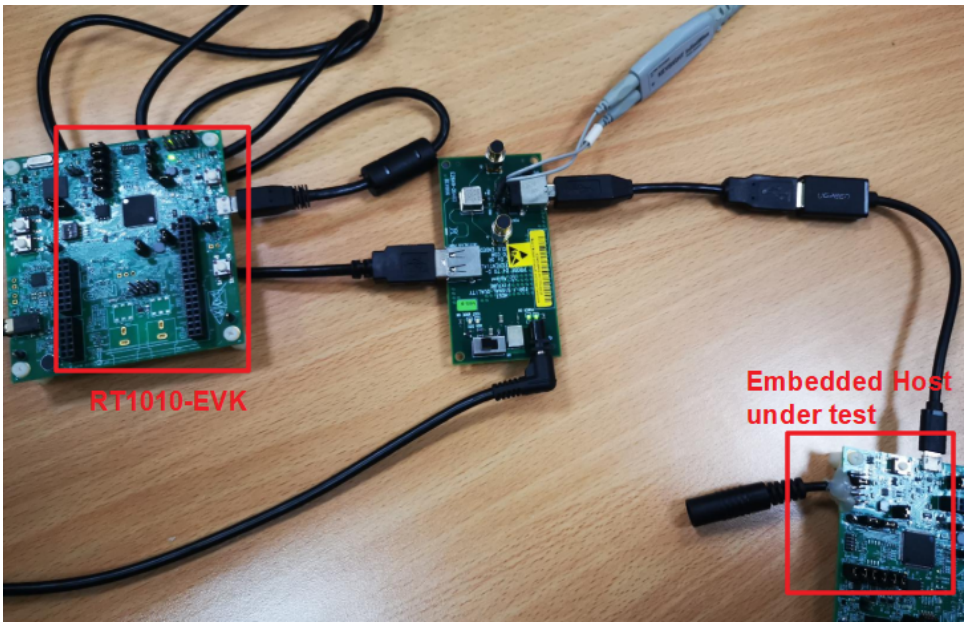

Figure 41. Embedded Host connection physical map

7. Click the **Run Tests** button of the automated test software on the oscilloscope. Enable the power to the Embedded Host under test and the MIMXRT1010-EVK. The host enumerates the RT1010-EVK board and responds to send `Test_Packet` continuously.
8. According to the prompt of the software on the oscilloscope, flip the switch of the test fixture that switches the termination on. Ensure that the yellow Test LED is lit. Confirm that the waveform oscilloscope catch is similar to the waveform prompted in the automated test software.

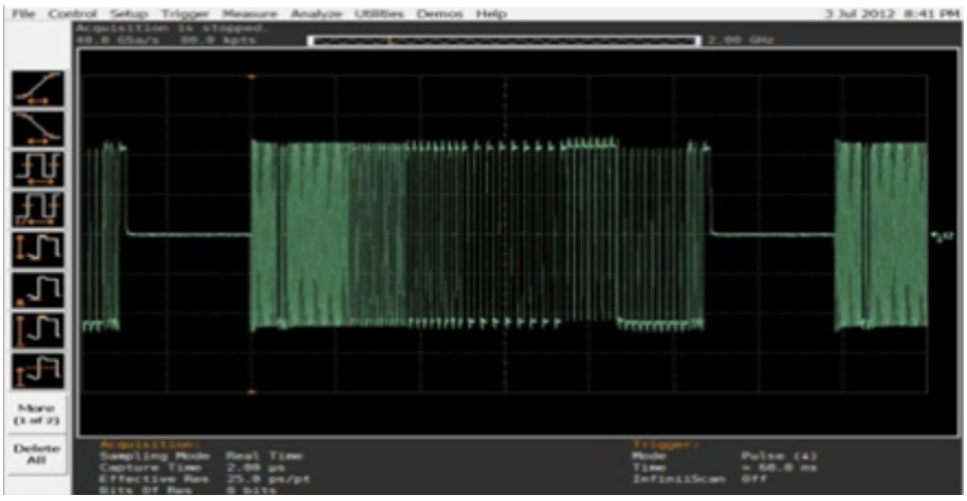

Figure 42. Prompted Host test packet waveform

9. When the **Testing Complete** dialog appears, click **OK** to finish the test.

3.1.2.2 Embedded Host Controller Packet Parameters test procedure

The equipment used in this test is same as Embedded Host High-Speed Signal Quality test, except that the 5 V power supply can be kept off all the time.

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 43. Connect the equipment and test fixture as shown in Figure 40. Connect the 50 ohm terminator to the SMA interface on the fixture.

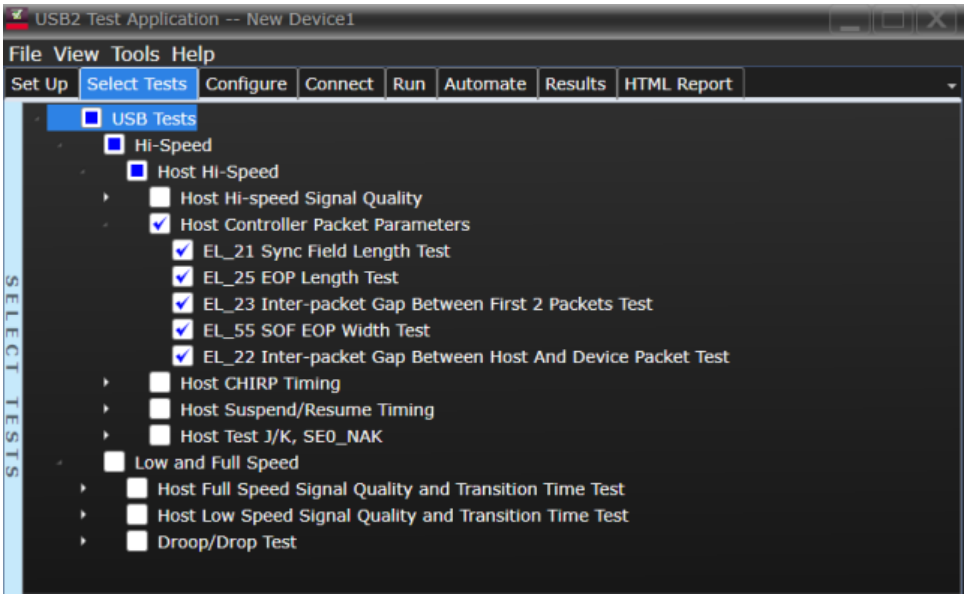

Figure 43. Embedded Host Controller Packet Parameters test

2. The connection of the embedded host under test, fixture, and oscilloscope probe is the same as the Signal Quality test.
3. Modify the PID of the demo to `0x0107`, re-compile, and download it to RT1010-EVK. Use a USB cable to connect the RT1010-EVK to the initialize port of the fixture.
4. Click the **Run Tests** button of the automated test software on the oscilloscope. The host enumerates the RT1010-EVK and responds to send SOFs for 15 seconds. Click **OK**.
5. After 15 seconds of SOFs the host initiates the setup phase of the `GetDescriptor()` command. The host sends **SETUP** and **DATA** (first and second packet). The device sends an **ACK**. The waveform that the oscilloscope catches is similar to the waveform prompted in the automated test software. Click **OK**.

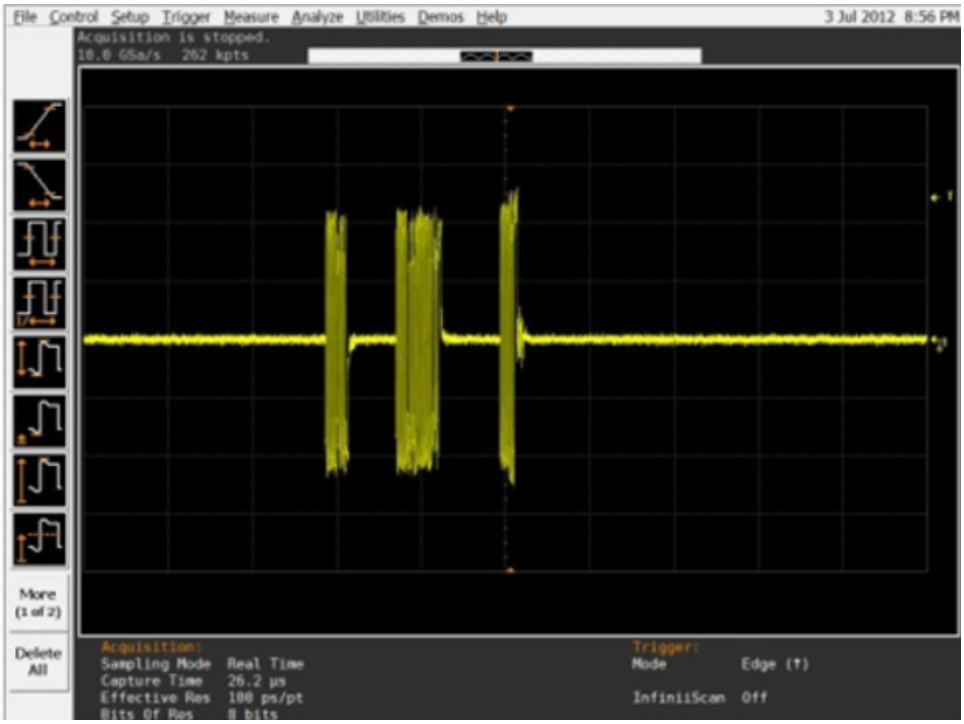

Figure 44. Prompted waveform

6. Disconnect the RT1010-EVK, modify the PID of the demo to `0x0108`, and download to the EVK again. Reconnect it to the test fixture.
7. The host enumerates the PID/VID, request `GetDescriptor()`, and waits for 15 seconds. The host issues an **IN**, the device responds with a **DATA**, and then the host sends an **ACK**. The oscilloscope catches the three packets and the waveform is similar to the waveform prompted in the automated test software. Click **OK**.

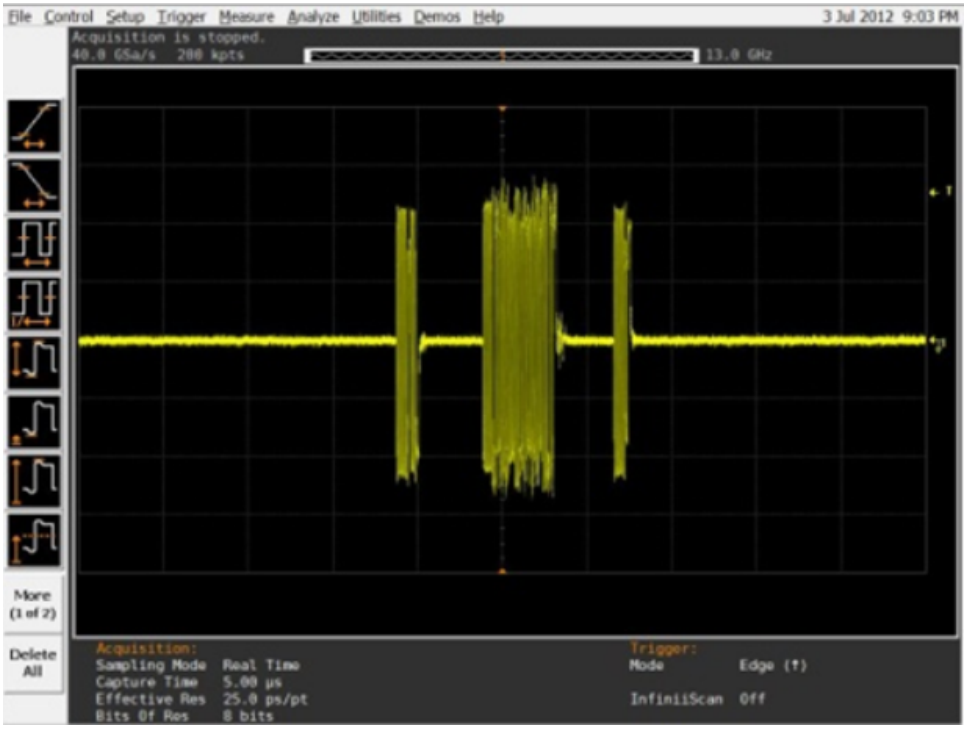

Figure 45. Prompted waveform

3.1.2.3 Host CHIRP Timing Test procedure

Table 11 lists the equipment used in the Host CHIRP Timing test.

Table 11. Equipment used in Host CHIRP Timing test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Single-ended probe	Keysight N2873A	2
PIDVID board	MIMXRT1010-EVK simulated	1
Host Hi-Speed Signal Quality test fixture and 4" USB cable	Keysight E2649-66402	1
5 V power supply	Keysight 0950-2546 or equivalent	1
USB cable	Micro-B plug OTG cable	1

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 46.

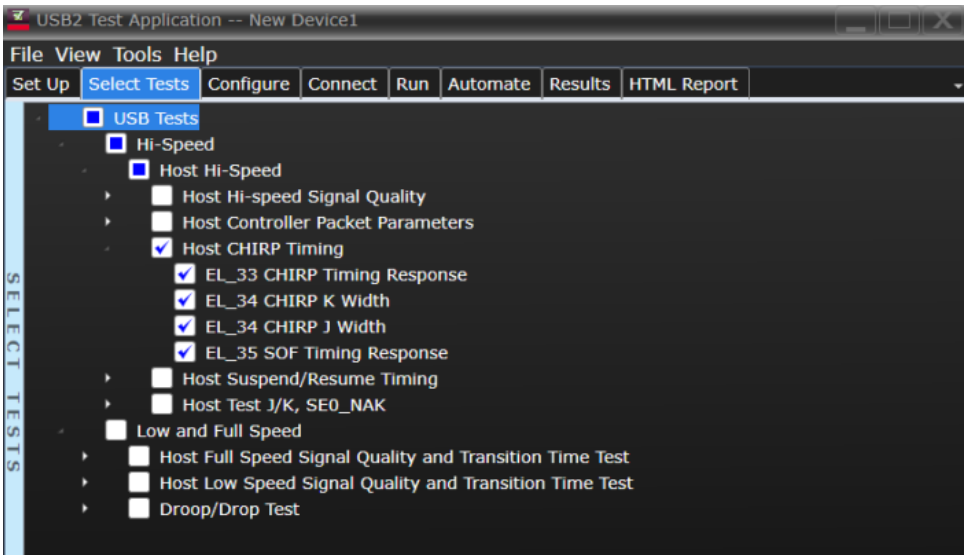

Figure 46. Host CHIRP Timing test

2. Connect the test-embedded host board, fixture, and oscilloscope, as shown in Figure 47. Connect the 50 ohm terminator to the SMA interface on the fixture. Verify that the switch in the fixture is OFF, the green Power LED is lit, and the yellow test LED is not lit.

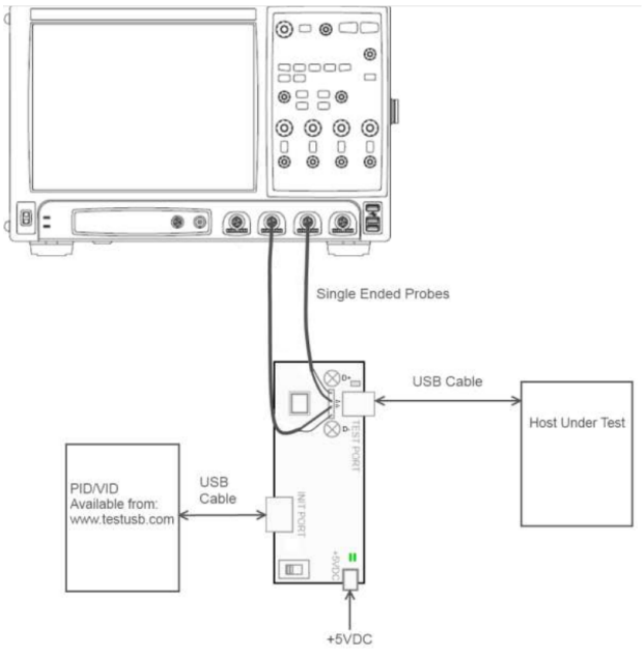

Figure 47. Host CHIRP Timing test connection

3. Connect any known good high speed device to the initialize port.
4. Click the **Run Tests** button of the automated test software on the oscilloscope. The oscilloscope captures the CHIRP handshake. The waveform is similar to the waveform prompted in the automated test software. Click **OK** to finish the test.

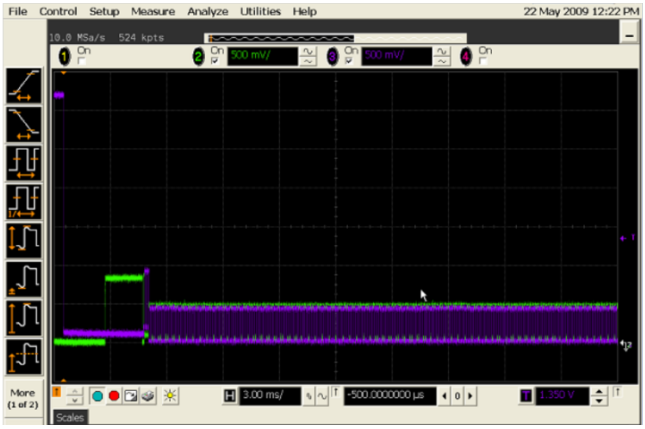

Figure 48. Prompted Host CHIRP waveform

3.1.2.4 Host Suspend/Resume Timing Test procedure

The equipment used in this test is the same as Host CHIRP Timing test, as shown in Table 11.

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 49.

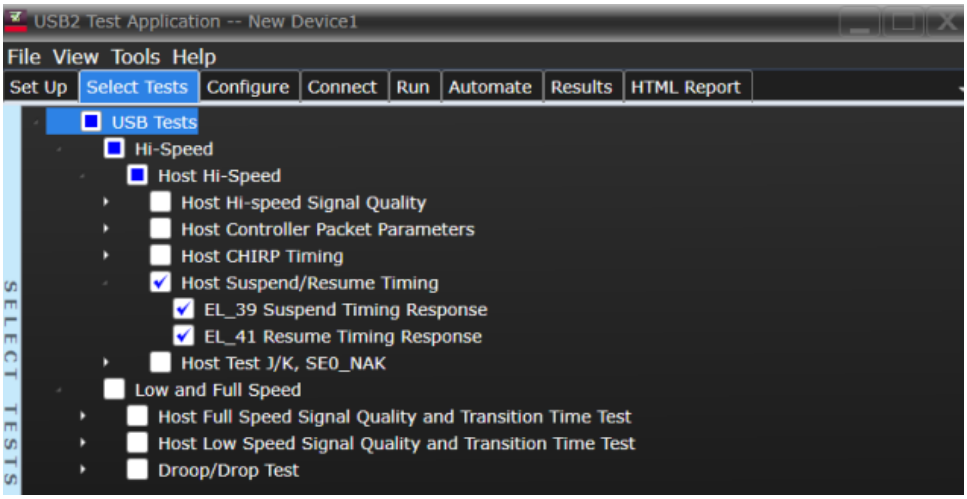

Figure 49. Host Suspend/Resume Timing test

2. Connect the test embedded host board, fixture, and oscilloscope, as shown in Figure 47. Connect the 50 ohm terminator to the SMA interface on the fixture. Verify that the switch in the fixture is OFF, the green Power LED is lit, and the yellow test LED is not lit.
3. Modify the PID of the demo to `0x0106`. Compile and download to RT1010-EVK again. Reconnect it to the test fixture.
4. Click the **Run Tests** button. After 15 seconds, the host port enters the Suspend state. The captured transition is similar to the prompt in the automated test software. Click **OK**.

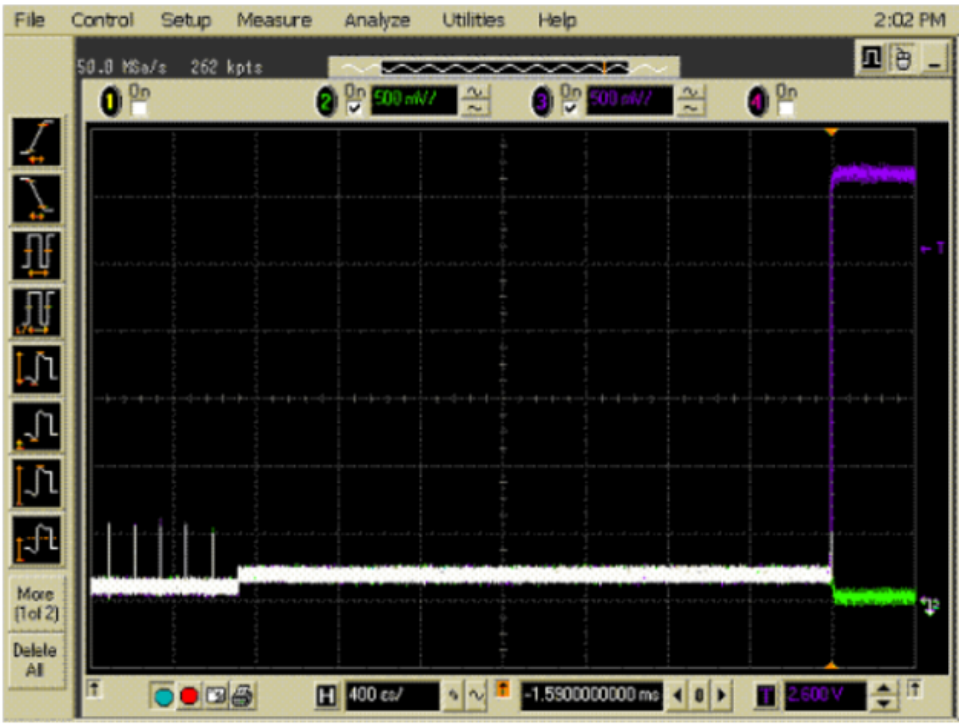

Figure 50. Prompted Host suspend waveform

5. After 15 seconds in the suspend state, the host issues a **ResumeK** state on the bus and then continues sending SOFs. The waveform that the oscilloscope captures is similar to the waveform prompted in the automated test software. Click **OK** to finish the test.

Figure 51. Prompted Host resume waveform

3.1.2.5 Host Test J/K, SE0_NAK test procedure

Table 12 lists the equipment used in the Host Test J/K, SE0_NAK test.

Table 12. Equipment used in Host Test J/K, SE0_NAK test

Item	Model	Quantity
Multimeter	Any	1
PIDVID board	MIMXRT1010-EVK simulated	1
Host Hi-Speed Signal Quality test fixture and 4" USB cable	Keysight E2649-66402	1
5V power supply	Keysight 0950-2546 or equivalent	1
USB cable	Micro-B plug OTG cable	1

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 52.

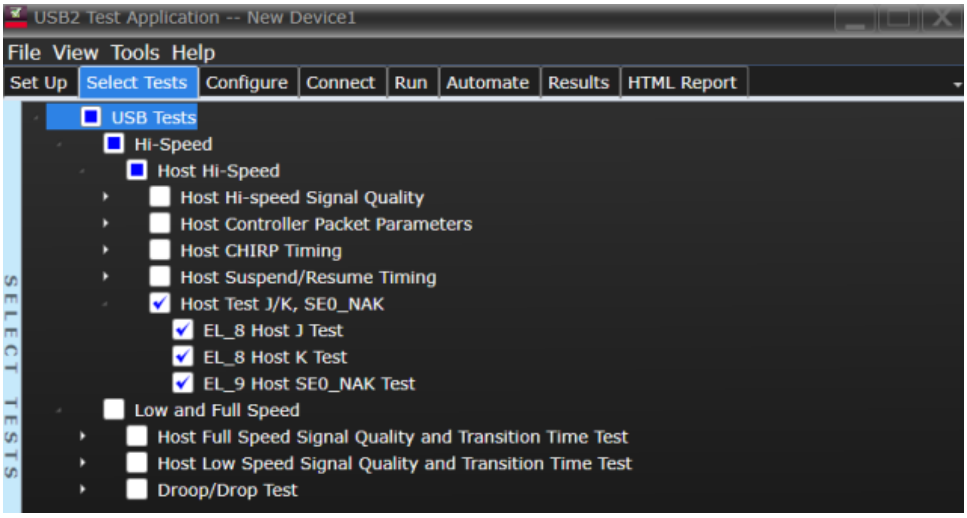

Figure 52. Host Test J/K, SE0_NAK test

2. Connect the test embedded host board and the fixture, as shown in Figure 53. Connect the 50 ohm terminator to the SMA interface on the fixture. Verify that the switch in the fixture is OFF, the green Power LED is lit, and the yellow Test LED is not lit.

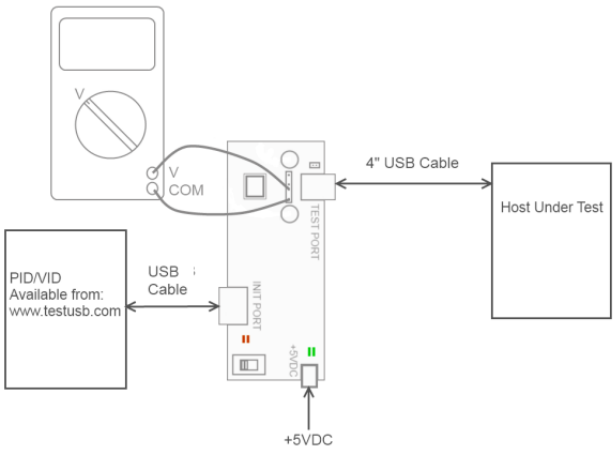

Figure 53. Host Test J/K, SE0_NAK test connection

3. Click the **Run Tests** button of the automated test software on the oscilloscope.
4. Modify the PID of the demo to `0x0102`. Compile and download it to RT1010-EVK again. Reconnect it to the test fixture.
5. The host enumerates the RT1010-EVK and enters a high-speed J state (D+ high; D- low).
6. According to the prompt of the software, flip the switch of the test fixture that switches the termination on. Ensure that the yellow test LED is lit. Use a multimeter to measure the DC voltage on the D+/D- lines at TP2 with respect to GND. Record the measurement in the pop out dialog on the oscilloscope. Click **OK**.
7. Flip the test switch to OFF. Reset the power to the embedded host board under test.
8. Disconnect RT1010-EVK board. Modify the PID of the demo to `0x0103`. Compile and download it to RT1010-EVK again. Reconnect it to the test fixture.
9. The host enumerates the PID/VID and enters a high-speed K state (D+ low; D- high).
10. According to the prompt of the software, flip the switch of the test fixture that switches the termination on. Ensure that the yellow test LED is lit. Use a multimeter to measure the DC voltage on the D+/D- lines at TP2 with respect to GND. Record the measurement in the pop-up dialog on the oscilloscope. Click **OK**.
11. Flip the test switch to OFF. Reset the power to the embedded host board under test.
12. Disconnect RT1010-EVK board. Modify the PID of the demo to `0x0104`. Compile and download it to RT1010-EVK again. Reconnect it to the test fixture.
13. Flip the switch of the test fixture that switches the termination on. Ensure that the yellow Test LED is lit. Use a multimeter to measure the DC voltage on the D+/D- lines at TP2 with respect to GND. Record the measurement in the pop-up dialog on the oscilloscope. Click **OK** to finish the test.

3.1.3 Full-Speed and Low-Speed signal test

Low and Full Speed items include：

- For Device
  - Upstream Full Speed Signal Quality Test
  - Back-Voltage Test
  - Device Inrush Current Test
- For the host
  - Downstream Full Speed Signal Quality Test
  - Downstream Low Speed Signal Quality Test

— Host Drop Test

The i.MXRT series chips do not support the low-speed device, so the pre-test does not contain the Upstream Full-Speed Signal Quality Test.

3.1.3.1 Upstream Full-Speed Signal Quality Test procedure

Table 13 lists the equipment used in the Upstream Full-Speed Signal Quality Test.

Table 13. Equipment used in Upstream Full-Speed Signal Quality Test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Single ended probe	Keysight N2873A	3
SQiDD board	Keysight E2646B	1
USB self-powered hubs	Any listed on USB-IF website	5
5 meter USB cables	Any listed on USB-IF website	6

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 54.

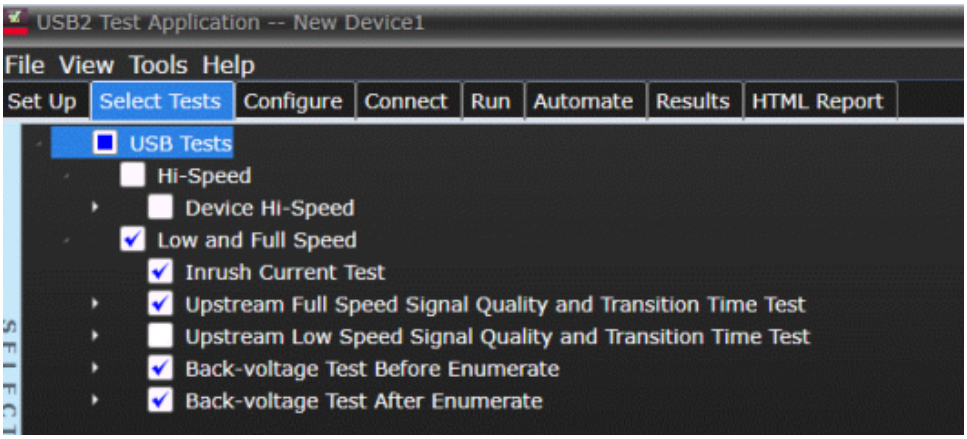

Figure 54. Upstream Full-Speed Signal Quality Test

2. Connect the equipment and test fixture as shown in Figure 55. Since the test is the signal quality of the Device's Upstream port, the upstream layer 5 hub has no effect on the signal integrity. Therefore, if you do not have enough hubs on hand during the pre-test, to force the Device to run at full speed, connect only one full speed hub. The obtained eye diagram is also credible.

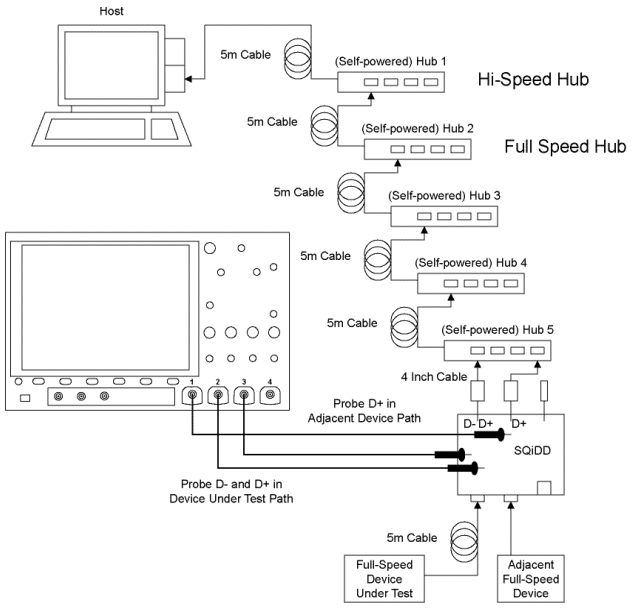

Figure 55. Upstream Full-Speed Signal Quality Test connection

3. Click **Run Tests** in the USB automated test software on the oscilloscope.
4. Similar to the High-Speed Signal Quality test, on the Device Test menu of the HS electrical test tool software, click **Enumerate Bus** once. Select the device under test in the device enumeration list, select **LOOP DEVICE DESCRIPTOR** from the Device Command drop-down menu, and click **Execute** once, as shown in Figure 56.

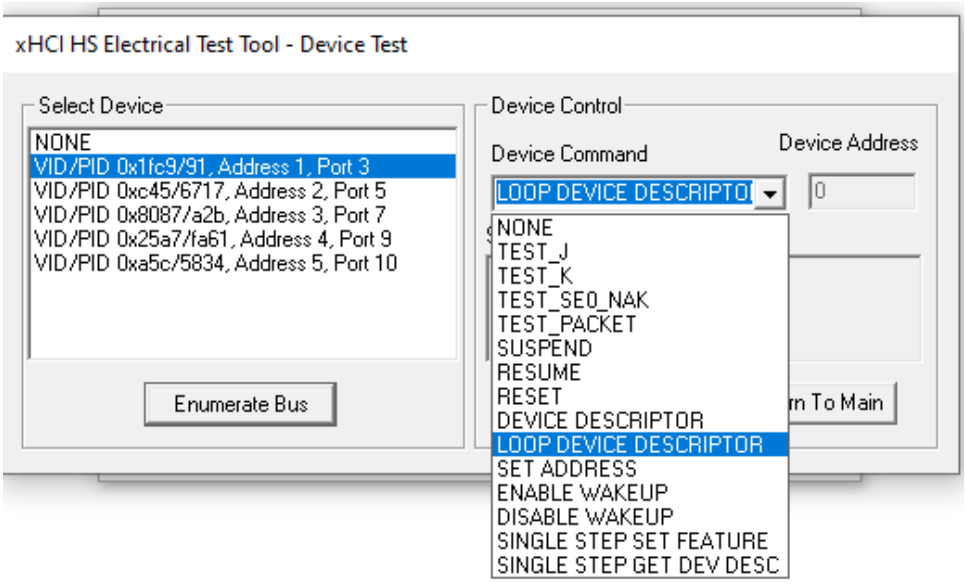

Figure 56. HSETT Loop Device Descriptor command

5. The oscilloscope captures the waveform. When the **Testing Complete** dialog appears, click **OK** to finish the test.

3.1.3.2 Back-Voltage test procedure

Use the multimeter and SQiDD board for the Back-Voltage test. All the voltages measured in this test must be less than or equal to 400 mV. Any voltages greater than 400 mV will be recorded as a failure.

To run the test, perform the following steps:

1. Select the test items in the USB Automated Test software on the oscilloscope as shown in Figure 54.
2. Use a known good USB cable to connect the power supply to the DUT and the device upstream port to the SQiDD board, as shown in Figure 57. Do not connect any Host. Click **Run Tests** in the USB automated test software on the oscilloscope.

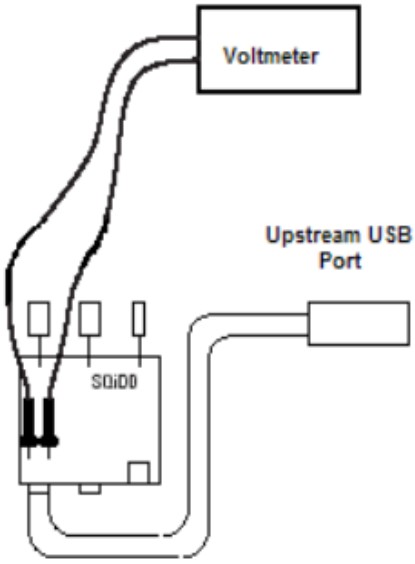

Figure 57. Back-Voltage Test connection

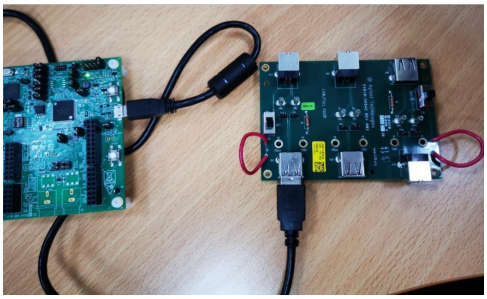

Figure 58. Back-Voltage physical map

3. Measure the DC voltages on Vbus, D+, and D-. Record them in the pop-up dialog on the oscilloscope. Click **OK**.
4. Plug the DUT into a known good host and verify proper enumeration. Unplug the USB cable from the host and reconnect the USB cable to the back-voltage test fixture.
5. Measure the DC voltages on Vbus, D+, and D- again. Record them in the pop-up dialog on the oscilloscope. Click **OK** to finish the test.

3.1.3.3 Device Inrush Current Test procedure

The USB 2.0 specification support maximum capacity of 10 uF and therefore a maximum inrush of 50 uC. Measure Inrush current for a minimum of 100 ms after attachment. As there is not a Keysight current probe in hand, in this application note, use a Tektronix oscilloscope for the test. The model number is DPO2024B and the current probe model number is TCP0030A.

To run the test, perform the following steps:

1. When taking the measurement, calibrate the current probe to 0 mA. If not performed beforehand, a current probe produces a DC offset resulting in an incorrect measurement.
2. Connect the equipment and test fixture, as shown in Figure 59. Use the current probe to capture the **Vbus** current waveform. Ensure that the probe direction is the same.

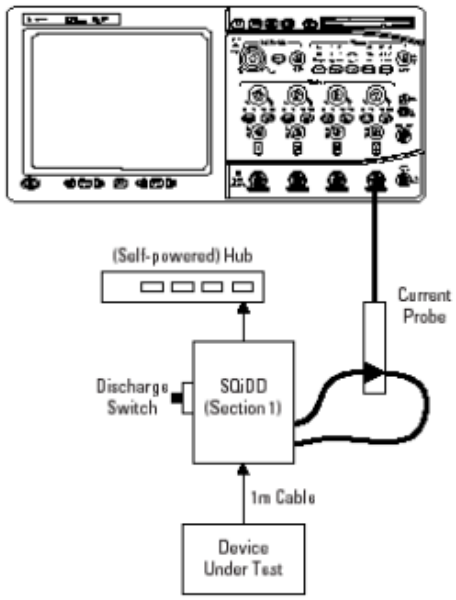

Figure 59. Device Inrush Current Test connection

3. Connect the device under test to the SQiDD board. Place the switch on the SQiDD board to the discharge position (opposite the ON position).
4. Set the oscilloscope as Single mode and the record length as 5 M which can match the requirement: time base 50 ms/div, vertical resolution 500 mA/div, sample rate >1MS/s.
5. Place the switch on the SQiDD board to the ON position. The oscilloscope captures the inrush current waveform and saves the waveform to the U-Disk as a `*.csv`.
6. Copy the `*.csv` file to PC. Open the file in the USBET20 software as shown in Figure 60. The file can be downloaded from USB-IF Document page. Click **Test**, and the result pops up.

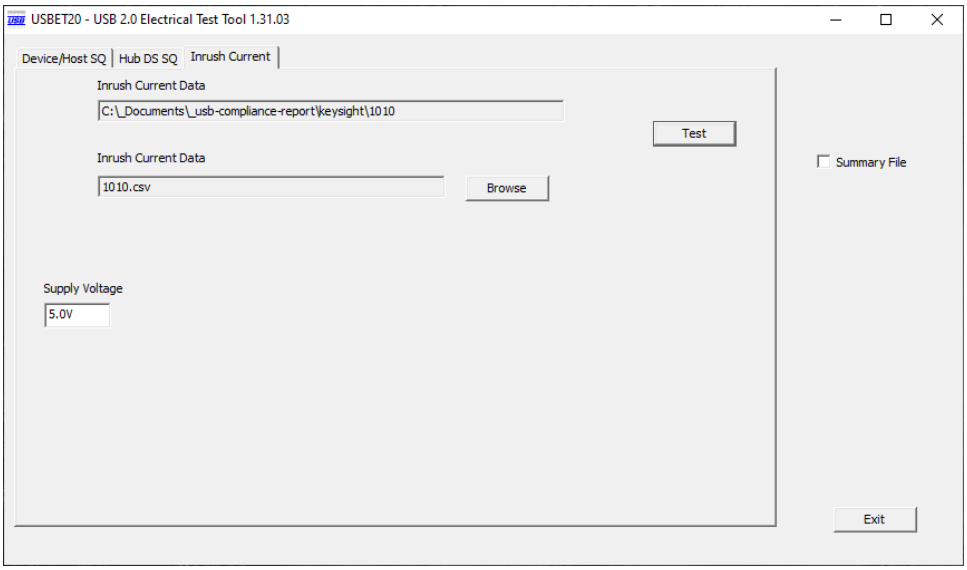

Figure 60. USBET20

3.1.3.4 Downstream Full-Speed Signal Quality Test procedure

Table 14 lists the equipment used in the Downstream Full-Speed Signal Quality Test.

Table 14. Equipment used in Downstream Full-Speed Signal Quality Test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Single ended probe	Keysight N2873A	2
SQiDD board	Keysight E2646B	1
Full speed USB device	Any	1
USB cable	Micro-B plug OTG cable	1

To run the test, perform the following steps:

1. Select the test items in the USB Automated Test software on the oscilloscope, as shown in Figure 61.

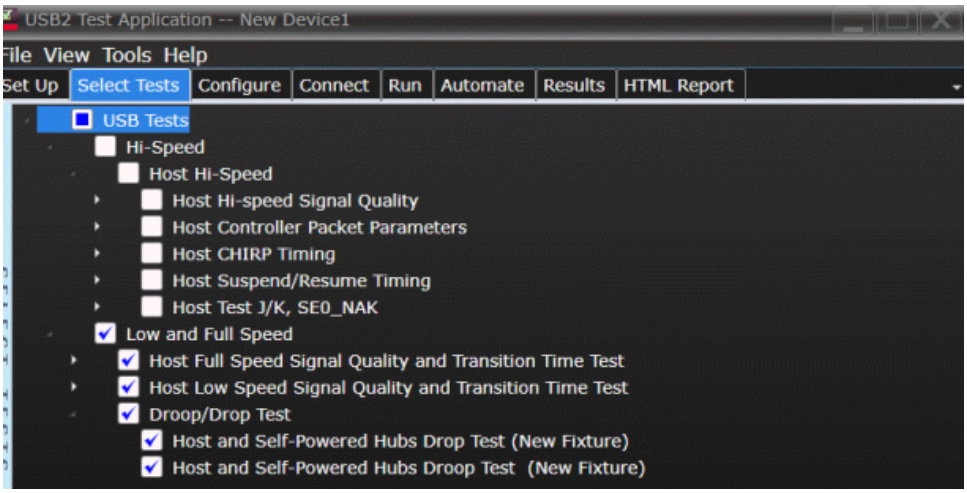

Figure 61. Downstream Full-Speed Signal Quality Test

2. Connect the Embedded Host under test, full speed device, and the SQiDD, as shown in Figure 62. Set the switch on SQiDD board to ON. The test is for the embedded host, so use the embedded host board to replace the PC in Figure 62.

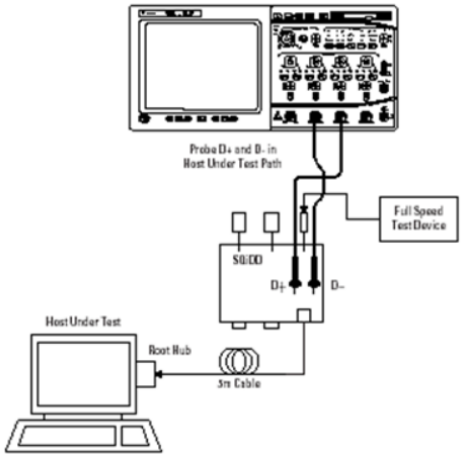

Figure 62. Downstream Full-Speed Signal Quality Test connection

3. Click **Run Tests** in the USB automated test software on the oscilloscope. When the **Testing Complete** dialog appears, click **OK** to finish the test.

3.1.3.5 Downstream Low-Speed Signal Quality Test procedure

Table 15 lists the equipment used in the Downstream Low-Speed Signal Quality Test.

Table 15. Equipment used in Downstream Low-Speed Signal Quality Test

Item	Model	Quantity
Oscilloscope	Keysight DSOS604A	1
Single ended probe	Keysight N2873A	2
Low speed USB device	Dell mouse	1

Table continues on the next page...

Table 15. Equipment used in Downstream Low-Speed Signal Quality Test (continued)

Item	Model	Quantity
SQiDD board	Keysight E2646B	1
USB cable	Micro-B plug OTG cable	1

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 61.
2. Connect the Embedded Host under test, mouse, and the SQiDD, as shown in Figure 63. Set the switch on SQiDD board to ON. The test is for Embedded Host, so use the Embedded Host board to replace the PC in Figure 63.

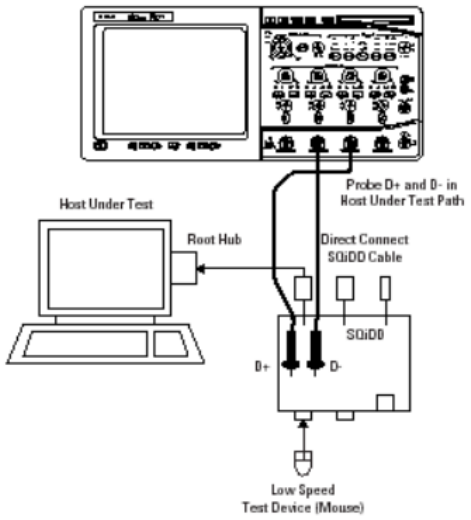

Figure 63. Downstream Low-Speed Signal Quality Test connection

3. Click **Run Tests** in the USB automated test software on the oscilloscope. When the **Testing Complete** dialog appears, click **OK** to finish the test.

3.1.3.6 Host Drop Test procedure

To host full-load current, the drop test measures a host/hub's ability while keeping the output voltage above specification. To perform this test, measure V_{bus} with all downstream ports loaded with 500 mA loads (for host and self-powered hubs). The lowest value measured across all ports must be between 4.75 V and 5.5 V1 for host and self-powered hubs.

The Droop test is a transient test on adjacent ports. When a device is hot plugged into another port, the droop in V_{bus} supplied to a port must be less than or equal to 330 mV for host, self-powered, and bus-powered hubs. There is only one port for the embedded host, so this test is not needed.

Table 16 lists the equipment used in the Host Drop Test.

Table 16. Equipment used in Host Drop Test

Item	Model	Quantity
Computer or USB power adapter	Any computer with USB ports or USB power adapter	1
Multimeter	Any	1

Table continues on the next page...

Table 16. Equipment used in Host Drop Test (continued)

Item	Model	Quantity
Droop Drop test fixture	Keysight E2649-66405	1
USB cable	Micro-B plug OTG cable	1

To run the test, perform the following steps:

1. Select the test items in the USB automated test software on the oscilloscope, as shown in Figure 61. Switch to **Set Up** tab and select **Keysight Droop Drop Fixture**.
2. Connect the **J11** of the test fixture to the USB port of the PC or the USB power adaptor to power the fixture. The green LED DS1 is lit.
3. Flip the switch S5 to **Drop Test** and switch S4 to 500 mA. Press and hold **S1** until the 7-segment LED test port indicator lights up. The test fixture is now turned on. U7 illuminates with a zero, indicating the initial state. This means the Port 0 is the test port.
4. Connect J3 to the USB port of the Embedded Host under test. Measure V_{bus} and record it as $V_{non\text{-}load}$.
5. Press **S1**. While holding it down, press S2, measure the V_{bus}, and record it as V_{load}.
6. Fill in these two values to the pop-up dialog of the oscilloscope to finish the test.

3.2 Device Framework test

To test a USB device or hub, test the USBCV (Command Verifier). It automatically tests the device framework and the descriptor. It tests the standard commands in Chapters 9 and 11 of the USB 2.0 specification. Depending on the controller of the test host, the CV test contains USB20CV and USB30CV. As the PC with EHCI is not in hand, this application note just performs the USB30CV test. USB20CV test items are same as USB30CV.

Some software tools are required for the CV test. USB 3 GEN X CV can be downloaded from USB-IF Document page.

Device Framework pre-test items include:

- USBCV Chapter 9 Test
- USBCV Class Test

3.2.1 USBCV Chapter 9 test

Chapter 9 test covers the device support of the commands set in Chapter 9 of the USB specification.

To run the test, perform the following steps:

1. Connect the device under test to the test bed computer, open the USBCV software, and let the software control the USB controller of the computer. All standard peripherals on your computer such as mouse and u-disk are invalid at this moment. Figure 64 shows the interface of the USBCV software.

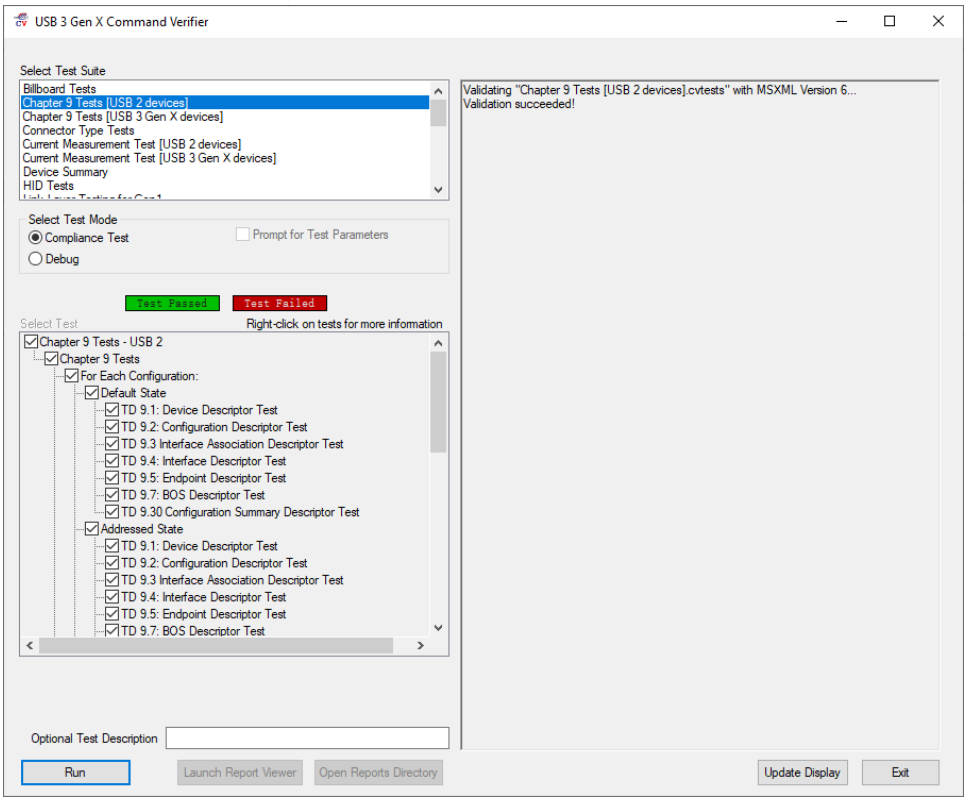

Figure 64. CV test interface

2. Select **Chapter 9 Tests[USB 2 devices]** and click **Run**. Select the device under test in the pop-up dialog, as shown in Figure 65. Click **OK** to run the test.

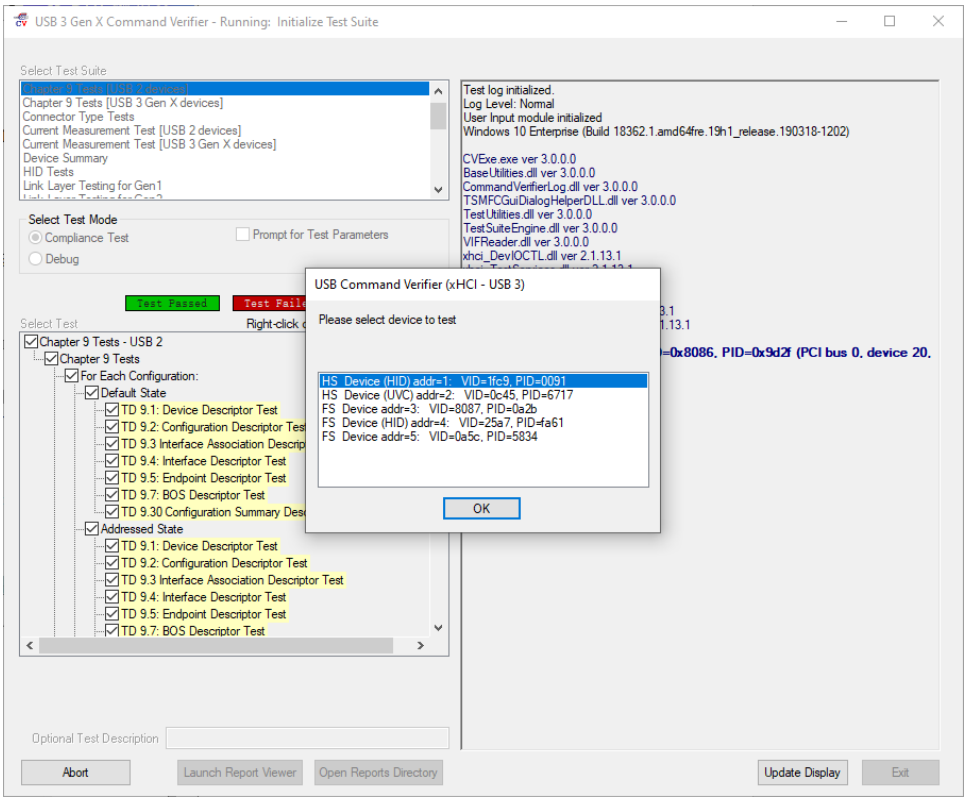

Figure 65. Selecting test device

3. The software performs all test items automatically. The test result is printed in the dialog box on the right. When the test finishes, click **Launch Report Viewer** to see the report.
4. To make the device run in full speed, add a Full-Speed Hub between the device under test and the PC. Repeat the test.

3.2.2 USBCV Class test

Run appropriate class tests (HID, HUB, MSC, UVC, PHDC) according to the prompt of Chapter 9 tests, as shown in Figure 66. The device under test in this application note uses the USB HID Mouse demo, so just perform the HID test.

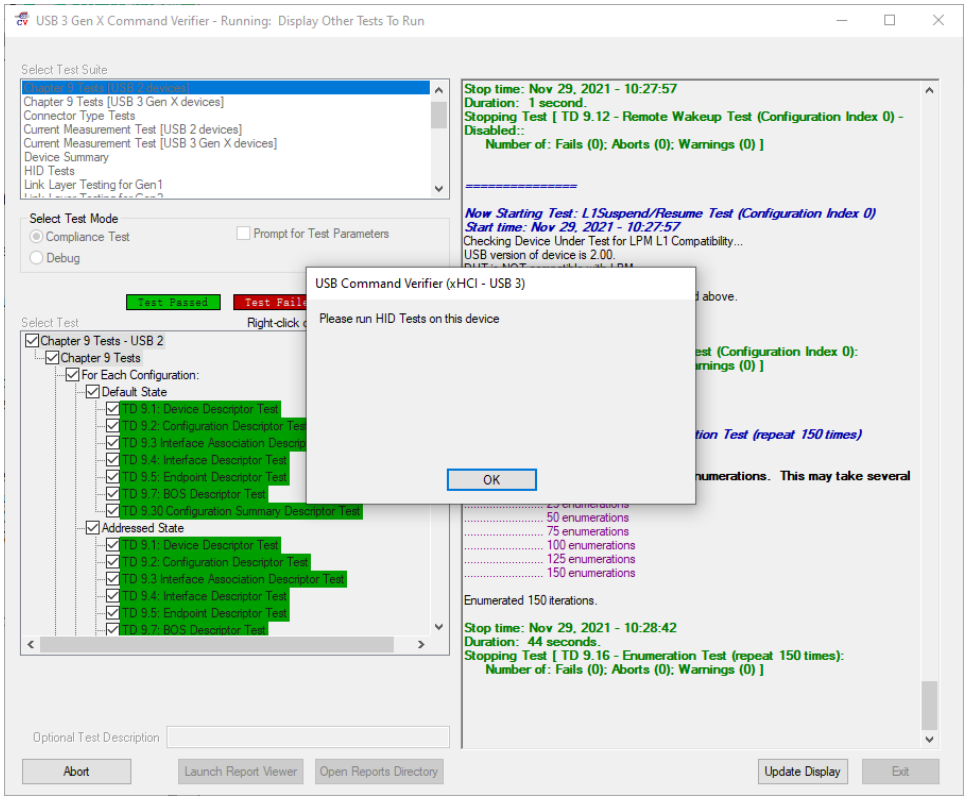

Figure 66. Prompt after Chapter 9 test

To run the test, perform the following steps:

1. Select **HID Tests** and click **Run**. Select the device under test in the pop-up dialog and click **OK** to run the test.
2. When the test finishes, click **Launch Report Viewer** to see the report.
3. To make the device run in full speed, add a Full-Speed Hub between the device under test and the PC. Repeat the test.

4 Notes and Failure items fix

4.1 Notes

4.1.1 Test software notes

Many test items in the pre-test of the USB compliance test need to use the PC, but the USB controller of most computers nowadays is xHCI. It is difficult to find a computer with EHCI controller. Therefore, for all software tool used in above tests, use the xHCI version. For example, for HSETT software, download the XHCI HSETT to perform the test; for CV software, use USB 3 GEN X CV software. In the formal laboratory test, the laboratory uses a host with EHCI to complete the EHCI part of the test.

If you cannot confirm the USB controller of the computer, get this information from the device manager. To open the **Computer Management** interface, right click **This PC**, choose, and click **Manage**. Click **Device Manager**, expand **Universal Serial Bus controllers** in the middle of the dialog box, as shown in Figure 67. Now, you can get the controller type of your computer.

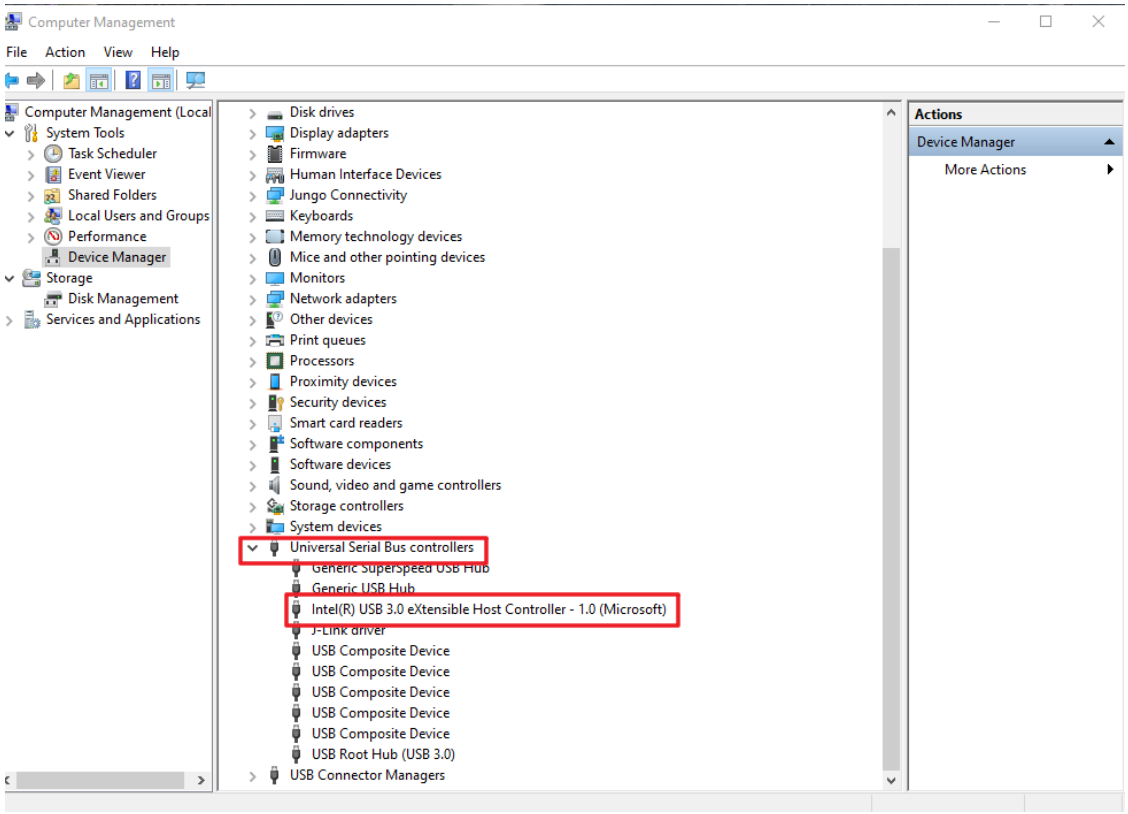

Figure 67. Controller type confirmation in computer

4.1.2 Configuration for test demo

The demo used in the device test is `usb_device_hid_mouse_bm`. This demo keeps the cursor moving on the screen. It may interfere with some functional tests. Therefore, modify the program in the `USB_DeviceHidMouseAction()` function before the test, as shown in Figure 68.

```
static usb_status_t USB_DeviceHidMouseAction(void)
{
    g_UsbDeviceHidMouse.buffer[1] = 0U;
    g_UsbDeviceHidMouse.buffer[2] = 0U;
    /* Send mouse report to the host */
    return USB_DeviceHidSend(g_UsbDeviceHidMouse.hidHandle, USB_HID_MOUSE_ENDPOINT_IN, g_UsbDeviceHidMouse.buffer,
                             USB_HID_MOUSE_REPORT_LENGTH);
}
```

Figure 68. Application code modification

The EVK board used for the pre-test does not have a battery. Disable the `USB_DEVICE_CONFIG_CHARGER_DETECT` macro in `usb_device_config.h` during the test. Otherwise, the laboratory performs the BC1.2 test. For the board without the battery, this test is not required.

When performing the interoperability test for the embedded host, use cascaded Hubs. To support the cascaded Hubs, define the `USB_HOST_CONFIG_HUB` value in the `usb_host_config.h` file of the `usb_host_msd_fatfs_bm` to 5.

4.1.3 Configuration for test hardware

The formal test of the certification laboratory contains a series of interoperability tests. For the interoperability test of Embedded Host, there are regulations on when V_{bus} power is supplied in the test items. As an embedded host, only when the ID pin is pulled low, the V_{bus} can be supplied. So when designing the hardware, use the design shown in Figure 69 to control the timing of V_{bus} power supply. Only when the ID line is pulled low, the power chip is enabled to supply power to V_{bus}.

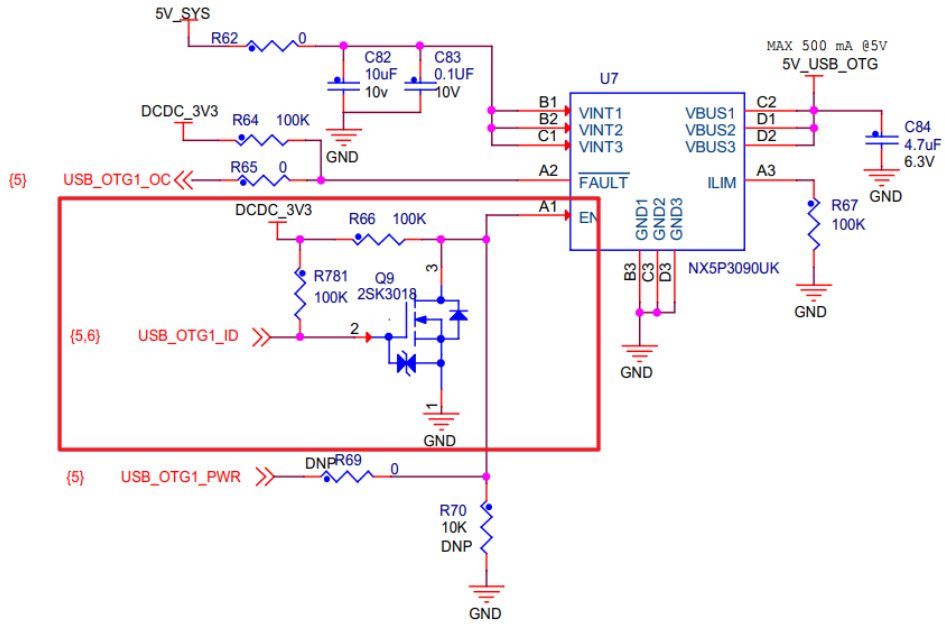

Figure 69. Power design for V_{bus}

4.2 Eye diagram adjustment

The signal quality test for the device and embedded host generates the eye diagram. In these tests, a failure may occur, as shown in Figure 70. This failure occurs because the drive capability of the transmitter is insufficient.

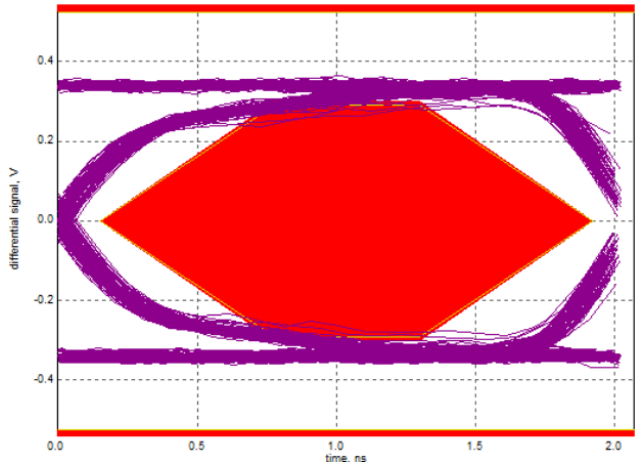

Figure 70. Failure eye diagram

Figure 71 shows a good eye diagram.

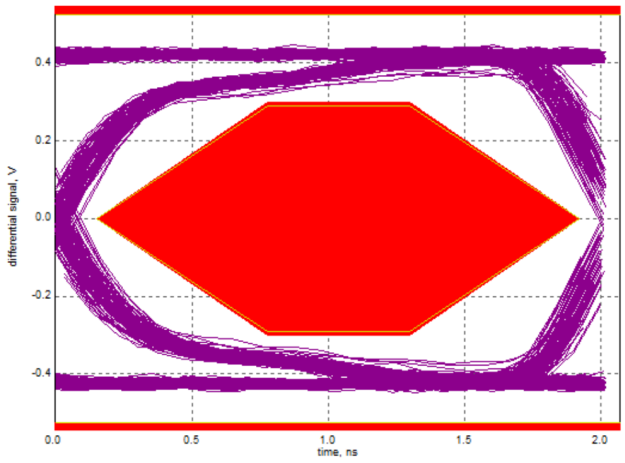

Figure 71. Good eye diagram

You can see that the in the good eye diagram, no data point violates the eye template which is the red area. For certification test, no data point violating the eye template is the standard to pass this test. The failure eye diagram is as shown in Figure 70, it have many data points violate the eye standard, how can we improve it?

The USB2.0 specification stipulates that the high-speed transmission adopts the current drive method, the current source, and the terminal resistance on the D+/D- line affect the drive capability of the transmitter.

To adjust the transmitter current source and the size of the terminal resistance on D+/D-, in the PHY of the RT series chips, there are three registers, `TXCAL45DP`, `TXCAL45DN`, and `D_CAL`. Table 17 describes the corresponding values of the specific register.

Table 17. Current source and terminal resistance adjustment

Field	Reset value	Description
TXCAL45DP TXCAL45DN	0110b	Adjust DP resistance Select a 45-Ohm resistance to the USB_DP output pin. Maximum resistance = 0000 0000 45+6*1.66 0001 45+5*1.66 0010 45+4*1.66 0011 45+3*1.66 0100 45+2*1.66 0101 45+1*1.66 0110 45 0111 45-1*1.66 1000 45-2*1.66 1001 45-3*1.66 1010 45-4*1.66 1011 45-5*1.66 1100 45-6*1.66

Table continues on the next page...

Table 17. Current source and terminal resistance adjustment (continued)

Field	Reset value	Description
		1101 45-7*1.66 1110 45-8*1.66 1111 45-9*1.66
D_CAL	0111b	Adjust the current of HS 0000 1.19*17.78mA 0001 1.16*17.78mA 0010 1.14*17.78mA 0011 1.12*17.78mA 0100 1.09*17.78mA 0101 1.06*17.78mA 0110 1.03*17.78mA 0111 1.00*17.78mA 1000 0.97*17.78mA 1001 0.95*17.78mA 1010 0.93*17.78mA 1011 0.90*17.78mA 1100 0.88*17.78mA 1101 0.86*17.78mA 1110 0.83*17.78mA 1111 0.79*17.78mA

As described in Table 17, D_CAL can adjust the value of the current source. If the eye diagram is not wide enough, reduce the value of the D_CAL and then test again. If the eye is still not wide enough, keep reducing the value of D_CAL until it has no data point violating the eye template. During the period, you can also modify the TXCAL45DP and TXCAL45DP to fine-tune the eye diagram. Vice verse, if the eye diagram spread too much, enlarge the value of D_CAL which can reduce the output of the current source, and then the eye diagram can open in a normal range.

For the failure in Figure 70, to increase the output current source, reduce the value of D_CAL according to Table 17 and then get the eye diagram again. Then, it can pass the test. The eye diagram test is the most important test in the HS Signal Quality Test. Modifying the three registers above does not interfere with the rest of the test.

4.3 Inrush Test failure

The test limit for Inrush current is that the maximum compliant inrush is 50 uC at 5 V. The maximum capacity is 10 uF. However, different PCB designs may make additional capacitance, so the Inrush test may fail. When the Inrush Current test fails, to pass the test, reduce the capacitance connected to V_{bus}. This capacitance cannot be completely removed. To make ADP detection possible, at least 1 uF of capacity is required.

4.4 Drop test failure

When performing the drop test on the embedded host, the voltage on the V_{bus} drops too much after the device is inserted. Used as a host, supply power to the inserted device. If the power supply of the host is insufficient, a large voltage drop occurs. When testing the embedded host, use a power adapter to supply the board.

5 Registering product in USB-IF

When the certification lab finishes all the test, submit your product to the USB-IF for registration to get the TID.

1. Check that your company is a member of USB-IF, register and log in to your account at https://groups.usb.org/site/login.
2. After logging in, click **Visit the Compliance Management Area** to enter the management interface. Click **Register USB Product**. Select a product type for your product, as shown in Figure 72. If you do not know what product type to choose, consult your test lab.

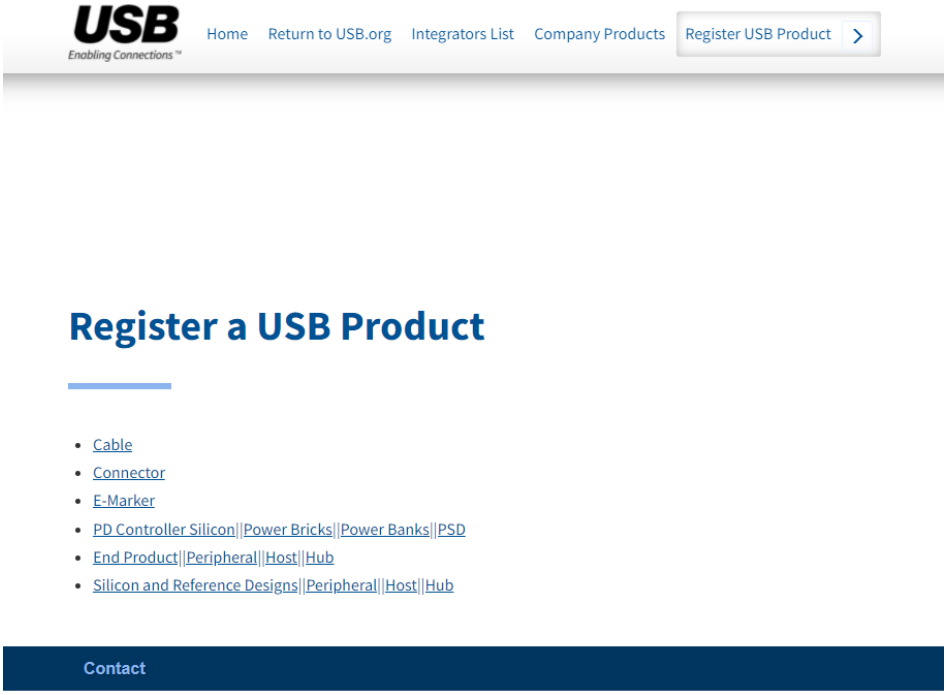

Figure 72. USB product type

3. Fill in the detailed information for your product, according to the guide that the certification lab sent to you to add the VIF file and the picture of the product.
4. After filling in all the information, click **Save**. The registered product is displayed in the **Company Products** menu.

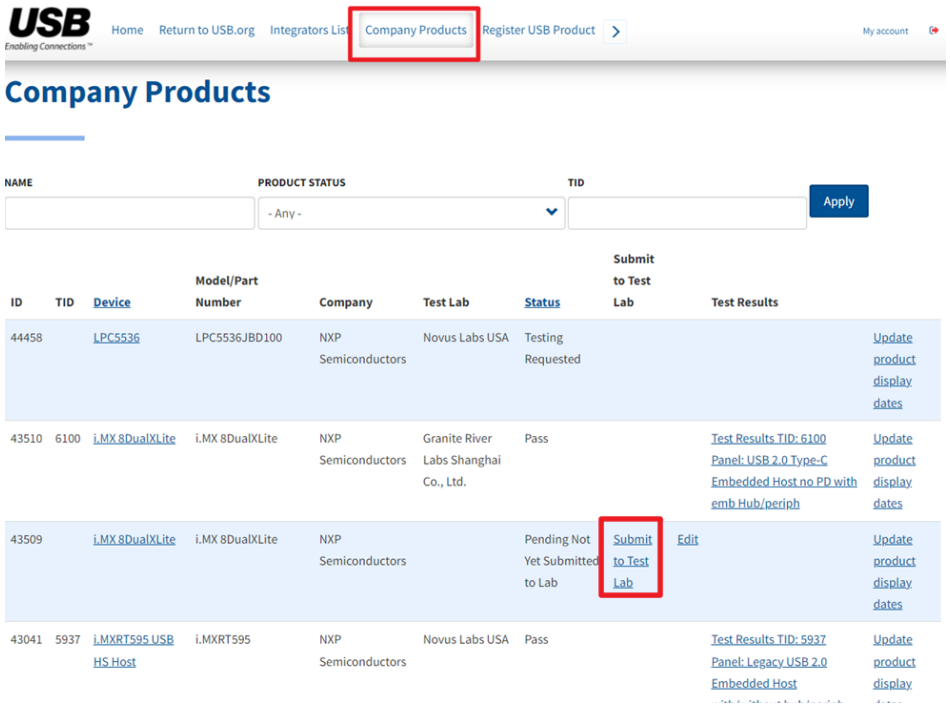

Figure 73. Company Products interface

5. Click **Submit to Test Lab** of your product, as shown in Figure 73. Choose the test lab on the test lab submission page.
6. Wait for the certification lab to upload the test result and wait for USB-IF to approve your product.

6 References

1. USB 2.0 Electrical Compliance Test Specification
2. Universal Serial Bus Implementers Forum Full and Low Speed Compliance Test Procedure
3. Embedded Host High Speed Electrical Test Procedure
4. Universal Serial Bus Revision 2.0 - USB Command Verifier Compliance Test Specification
5. Keysight D9010USBC USB 2.0 Compliance Test Application
6. i.MX6/7 Series USB Certification Guide

7 Revision history

Revision number	Date	Substantive changes
0	14 January 2022	Initial release

A Abbreviations

Term	Definition
HSETT	High Speed Electrical Test Tool
DUT	Device Under Test
EHCI	Enhanced Host Controller Interface(USB2.0)
xHCI	Extensible Host Controller Interface(USB3.0)
PID	Product Identification Number
VID	Vendor Identification Number
TID	Product Test ID assigned by USB-IF after passing the USB Certification Test
USB-IF	USB Implementers Forum

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