

AN13091

EV Traction Motor Power Inverter Control Reference Platform

Rev. 1 — 19 March 2021

Application note

1 Acronyms

Table 1. Acronyms

Acronym	Definition
PIM	Power Inverter Module
VCU	Vehicle Control Unit
ECU	Electronic Control Unit
TC	Traction Control
SDK	Software Development Kit
SBC	System Basis Chip
SPI	Serial Peripheral Interface
MCU	Micro-Controller Unit
IGBT	Insulated-Gate Bipolar Transistor
GD	Gate Driver
ASIL	Automotive Safety Integrity Level
RDC	Resolver-to-Digital Converter
SiC	Silicon Carbide
CMF	Common Mode Failure



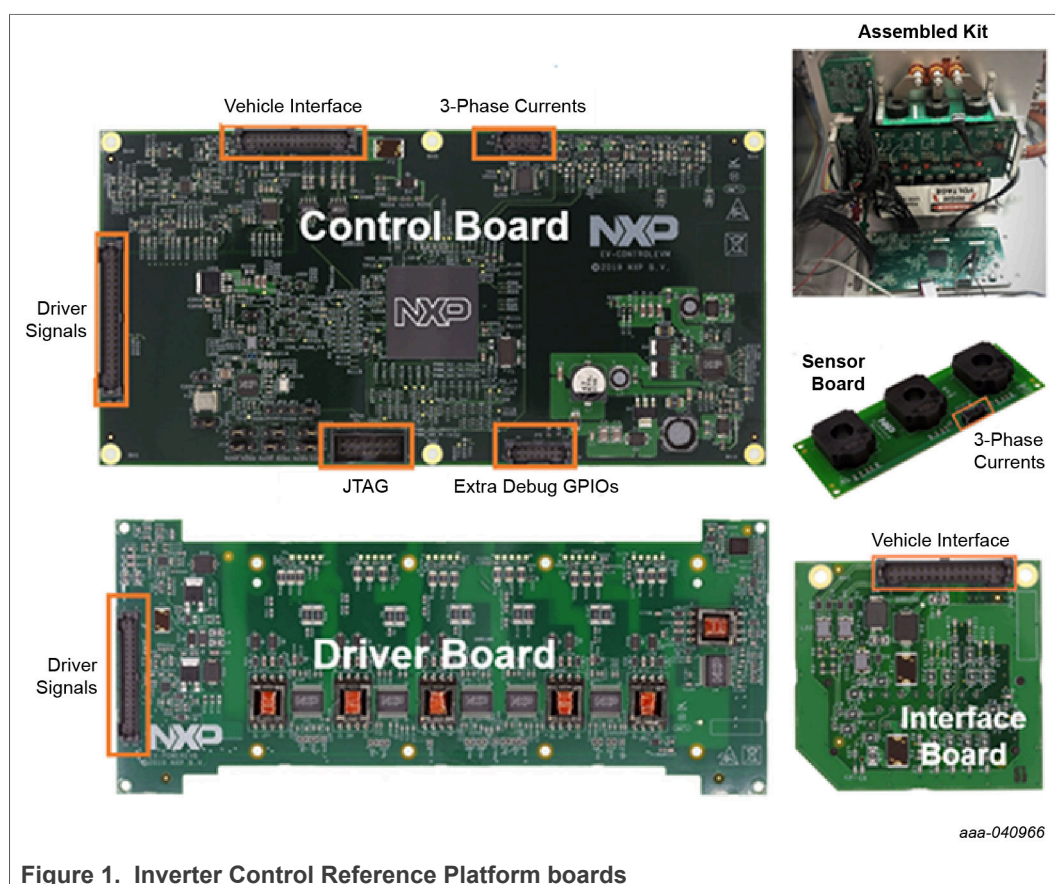
2 General Description

The NXP EV Power Inverter Control Reference Platform provides a hardware reference design, system basic software, and a complete system functional safety enablement as a foundation on which to develop a complete ASIL-D compliant high voltage, high-power traction motor inverter for electric vehicles.

The Reference Platform has been designed into an evaluation prototype demonstrating 150 kW peak output power and >96% electrical efficiency operating from a 320 V supply voltage.

The hardware reference platform is comprised of four boards:

- System control board
 - Same design and components apply when transitioning from IGBT to SiC
- Power stage driver board
 - GD3100 can be used for IGBT and SiC
- Current sensor board
- Vehicle interface board



System control board:

- This board contains three key NXP integrated circuits.
 - The MPC5775E is a 32-bit Power Architecture® dual core ASIL-D MCU targeted for motor control offering performance up to 264 MHz/core, CSE security, eTPU timers, software resolver, and a highly scalable solution.
 - The FS6500 system basis chip (SBC) providing power to the MCU optimizing energy consumption and providing low voltage side monitoring and protection.
 - The TJA1051 transceiver for high-speed CAN applications in the automotive industry providing differential transmit and receive capabilities to the MPC5775E and a CAN protocol controller.

Power stage driver board:

- This board is designed for the [Fuji M653 IGBT](#) module. It features the GD3100 advanced single-channel gate driver for IGBTs and SiC MOSFETs. Integrated galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage and rail-to-rail gate voltage control. The device autonomously manages severe faults and reports faults and status via an INTB pin and an SPI interface. Gate voltage is supplied via isolated transformers and a flyback controller.

This kit is designed to interface with a Fuji M653 IGBT module rated for 800 A / 750 V operation (purchased separately from Fuji Electronics).

The system basic software includes:

- Low-level SDK device drivers
- Software development abstraction layer
- System function service layer for simplifying customized motor control application software development on the reference control hardware

Optional:

- AMMCLIB (Advanced motor control function library)
- Platform functional safety management library (available in third quarter of 2021)

Featured NXP Components

- **GD3100** isolated high voltage IGBT/SiC gate driver with <2 μ s short-circuit protection
- **MPC5775E** advanced motor control ASIL-D MCU
- **FS65** robust ASIL-D Safe PMIC with fail-silent and Grade 0 capabilities
- **TJA1051T/3** redundant high-speed CAN bus interface

Features and functional safety benefits

- System control three-phase design kit for 100 kW class power inverters
- Efficient system BOM designed for ASIL-D safety requirements
- Basic highly optimized software enablement with inverter services layer, drivers and SDK
- $\pm 0.1^\circ$ high accuracy software resolver-to-digital converter (RDC) with advanced motor control software to eliminate external hardware interface for angle and speed calculation. Can also be used for redundant purposes
- Drives up to ± 15 A into a broad range of IGBT and SiC power devices
- <2 μ s iSense compatible two level IGBT OC protection with soft shutdown
- 5 kV galvanic signal isolation compatible with IGBTs up to 1700 V
- Standard signal interfaces for motor resolvers and output current sensors
- Redundant low and high side supply for the gate drivers for a high level of functional safety

- Multiple redundant circuits for fault monitoring of the gate driver failures to ensure a safe state
- Critical safety path to ensure availability of safe state
- Supports redundant CAN bus interfaces for VCU and for general purposes
- Operates from single 9 V to 16 V supply (customizable up to 36 V)
- Optional LDO (independent of FS65 SBC) powers low-side gate drivers in low-voltage domain for functional safety purposes

Applications

- EV motor power inverters
- High-voltage UPS power inverters
- Alternate energy power inverters

Additional Documentation

- Enablement Kit User Manual (UM11298)
- Basic software user manual (UM11317 - Available [here](#) with purchase of the kit)
- Safety application package (Available in third quarter of 2021)
- Hardware design package (schematics and layout) (Available [here](#) with purchase of the kit)
- System proof-of-concept prototype test results (Available [here](#) with purchase of the kit)

Reference Platform Conceptual Diagram

The Reference platform is made by three fundamental components:

- **Safety**
 - From the single components to the system level, to drastically reduce the effort of developing an ASIL-D system.
- **Hardware**
 - Efficient system BOM designed for ASIL-D safety requirements
- **Software**
 - Highly optimized and production-ready drivers to be used to as building blocks to implement any customer-specific motor control strategy.

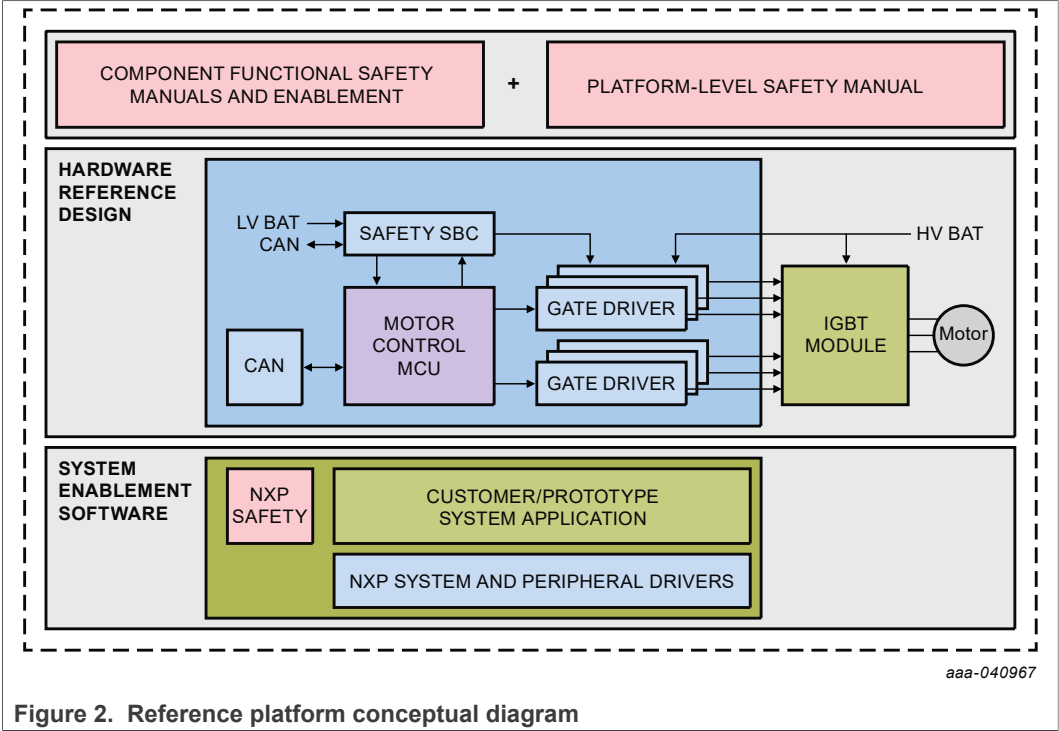


Figure 2. Reference platform conceptual diagram

3 Hardware and Software Block Diagram

3.1 Reference platform system overview

This reference design is a high-voltage inverter solution implemented for hybrid electric vehicle and electric vehicle traction control systems. It includes efficient system integration, protections, redundancies, enhanced safety and power flexibility to safely and efficiently drive the IGBT or SiC power modules.

[Figure 3](#) illustrates the platform architecture and highlights the hardware components. The isolated gate drivers galvanically isolate the high-voltage power supply from the low-voltage control signals.

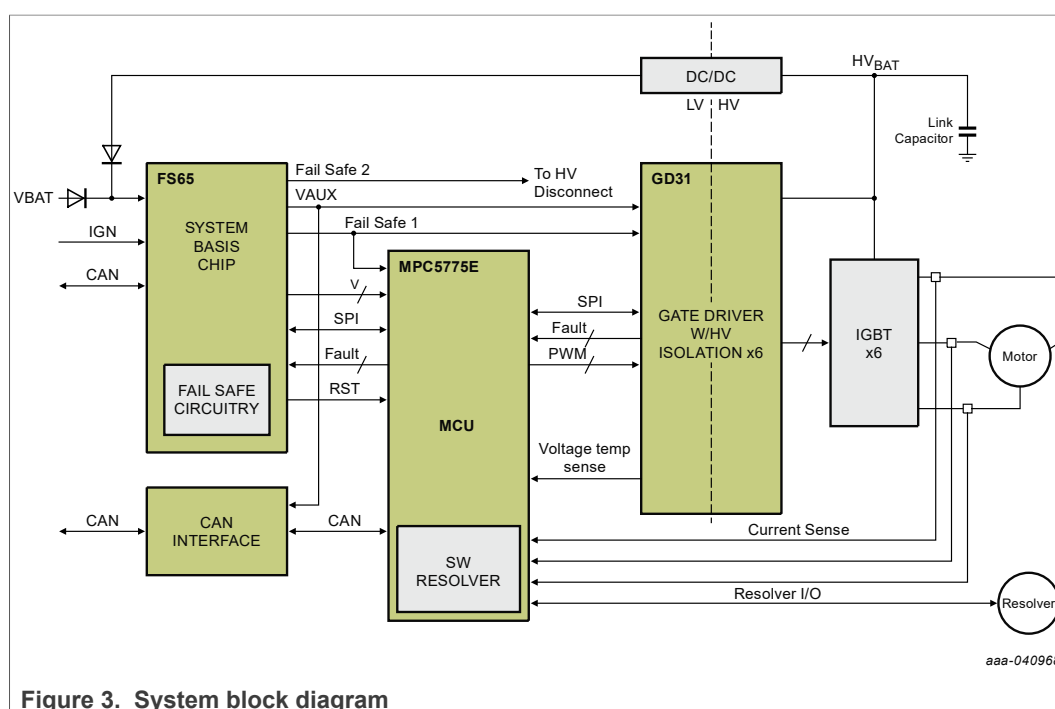


Figure 3. System block diagram

3.2 Inverter system basic software

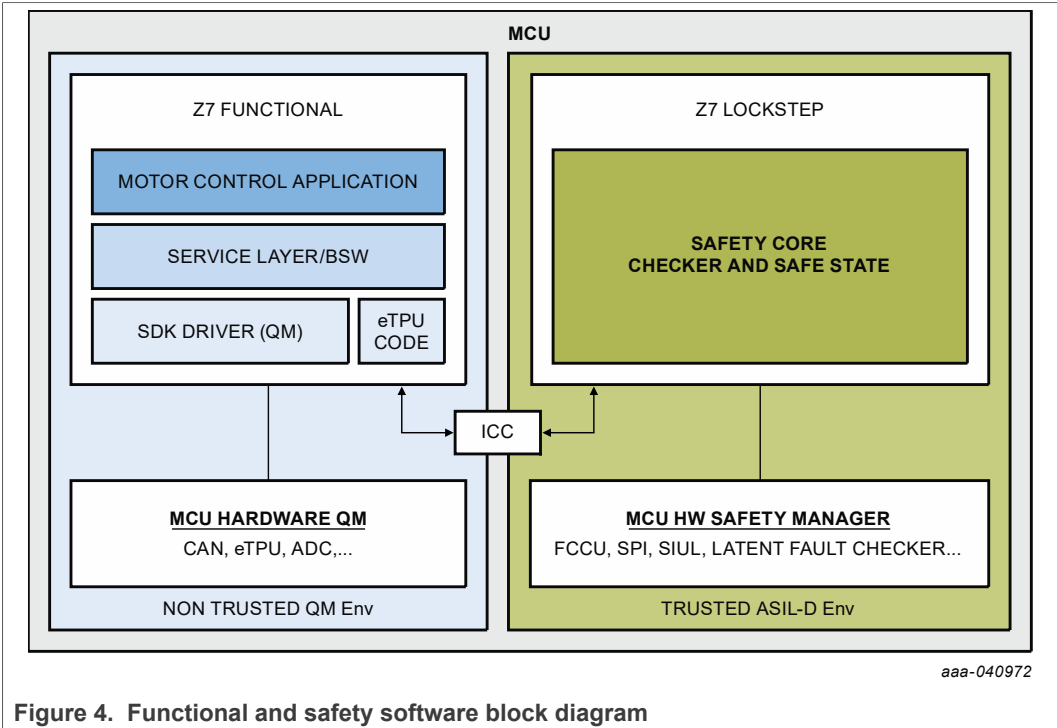
The Power Inverter Module (PIM) enablement software kit executes on the MPC5775E¹ MCU, which enables user-supplied motor control application software to control system configuration and operation through a set of API function routines and embedded basic motor control services.

A Software Development Kit (SDK) provides an easy to use environment for configuring the MCU abstraction layer and developing the motor control application software.

3.3 Software block diagram with optional functional safety enablement

[Figure 4](#) shows a high-level overview of system safety software that runs on a multi-core MCU. The safety critical software is executed on a lock-step CPU. All hardware safety measures are checked periodically against latent faults.

¹ The software is 100% compatible with MPC5777C



4 Platform System Architecture and Design

4.1 Reference platform hardware description

The inverter system platform architecture includes a MPC5775E advanced motor control 32-bit lock-step MCU that connects to six GD3100 isolated IGBT gate drive ICs and is supported by a FS65 safety and power management IC (SBC). The system block diagram in Figure 5 illustrates the architecture of the hardware components in the system.

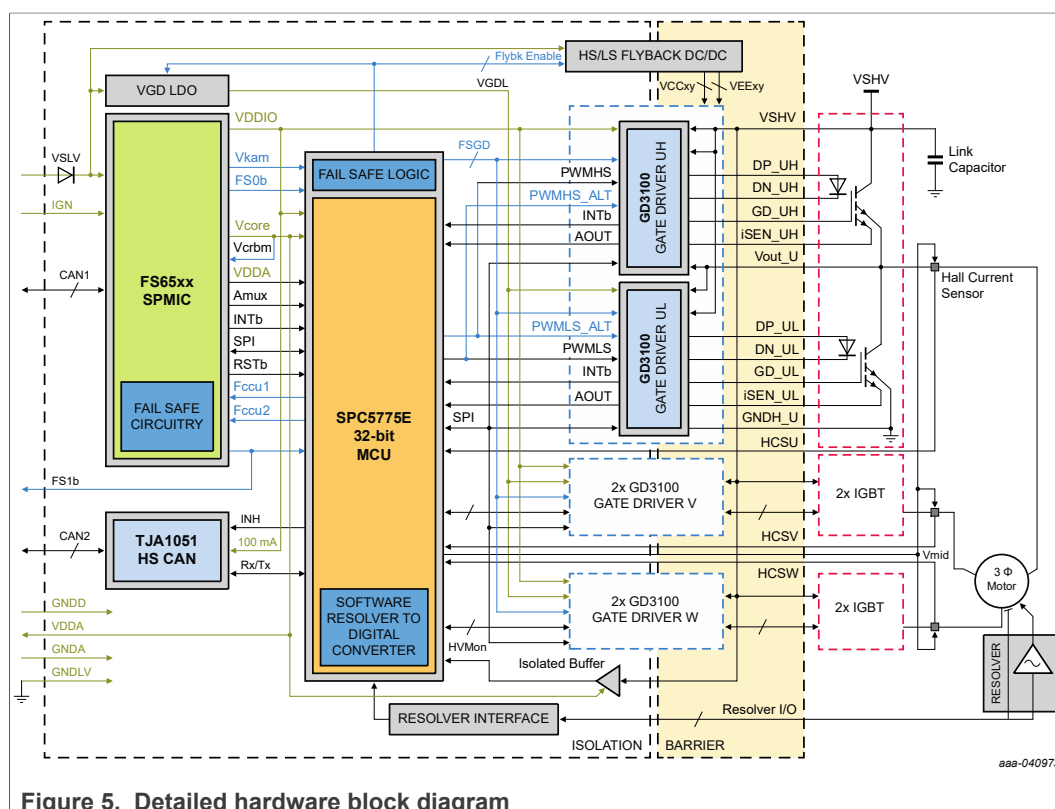


Figure 5. Detailed hardware block diagram

The MPC5775E is an ASIL-D compliant MCU, which is a high performance 32-bit Power Architecture microcontroller. There are three e200z7 host processor cores, two of which run in lockstep.

A system basis chip FS65 (SBC) provides power supply management, watchdog capabilities, fail-safe capability, and protected outputs to the MPC5775E. The SBC communicates with the MCU via SPI. The FS65 chip is compliant with ASIL D functional safety requirements (ISO 26262).

System communication is achieved with dual CAN bus interfaces, one integrated with the FS65 and connected to the vehicle control unit (VCU) (vehicle CAN) and one standalone TJA1051T/3 CAN transceiver (private CAN).²

The system platform is activated by a 5 V input signal that is detected by the FS65 IC and that subsequently powers up the other ICs in the platform and initializes system boot-up.

² Private CAN can be used for general purposes

For highest levels of functional safety, an optional LDO, independent of the FS65 SBC, supplies power to the low-side gate drivers on the low-voltage domain. On the high-voltage domain, the gate driver supply voltage is generated from a DC-to-DC fly-back voltage converter that boosts the main supply line voltage up to 15 V–18 V relative to the IGBT emitter voltages.

Three pairs of high-side and low-side IGBT gate driver (GD3100) output signal sets (U, V, W) interface to external IGBT power devices that in turn drive the three-phase inputs of the AC motor. Each GD3100 gate driver includes inputs for monitoring IGBT temperature, high-voltage supply level, IGBT desaturation, and IGBT integrated current sense cells (if available). An isolated buffer provides the MCU with fast feedback on the high-voltage supply level. The GD3100 autonomously manages severe faults and reports faults and status via the INTB pin and a SPI interface to the MCU. The GD3100 is capable of directly driving the gates of most IGBTs or SiC MOSFETs. Self-test, control, and protection functions are included for design of high reliability systems (ASIL/SIL).

Three sensor input signals connect Hall Current Sensor outputs directly to the MCU for monitoring the motor phase currents required for motor control. An output voltage reference from the MCU provides a mid-level voltage signal for use by the Hall Current Sensors. The platform also includes circuitry for interfacing the motor's resolver signals to the software resolver-to-digital converter in the MCU for detecting motor position required for motor control.

Inverter system enablement software running on the MCU enables user supplied motor control application software to control system configuration and operation through a set of API function calls and embedded basic motor control services. A Software Development Kit provides an easy to use environment for developing motor control application software.

4.2 Platform I/O

[Table 2](#) lists the Platform I/O. More details can be found in the Platform Hardware Design Package.

Table 2. Platform I/O

Name	Type	Description
VSLV	Analog In	Primary low-voltage power supply (12 V typical)
GND_LV	Ground	Low-voltage ground (return for 12 V supply)
GNDD	Ground	Digital Ground
CAN1H	Analog IN/OUT	CAN1 output high
CAN1L	Analog IN/OUT	CAN1 output low
CAN2H	Analog IN/OUT	CAN2 output high
CAN2L	Analog IN/OUT	CAN2 output low
IGN	Analog In	Inverter system activation input (K15)
FS1b	Analog Out	Fail-safe output (active low, open drain structure) asserted low at start-up and when a fault condition is detected, with a configurable delay or duration versus internal FS0B Fail-safe control signal.
VSHV	Analog In	High-voltage power supply
GNDH_x	GROUND	3x high-voltage ground signals for gate driver pair 'x' = U, V, W

Table 2. Platform I/O...continued

Name	Type	Description
Vout_x	Analog In	3x output signals for gate drive pair 'x'= U, V, W
GD_xH	Analog Out	3x High-side IGBT gate drive output for gate driver pair 'x'= U, V, W
GD_xL	Analog Out	3x Low-side IGBT gate drive output for gate driver pair 'x'= U, V, W
DP_xH	Analog IN/OUT	3x High-side IGBT diode P side connection for gate driver pair 'x'= U, V, W
DN_xH	Analog IN/OUT	3x High-side IGBT diode N side connection for gate driver pair 'x'= U, V, W
DP_xL	Analog IN/OUT	3x Low-side IGBT diode P side connection for gate driver pair 'x'= U, V, W
DN_xL	Analog IN/OUT	3x Low-side IGBT diode N side connection for gate driver pair 'x'= U, V, W
iSEN_xH	Analog In	3x High-side IGBT iSense input for gate driver pair 'x'= U, V, W
iSEN_xL	Analog In	3x Low-side IGBT iSense input for gate driver pair 'x'= U, V, W
HCSx	Analog In	3x Hall current sensor input for gate driver pair 'x'= U, V, W
Vmid	Analog	Mid point of the supply voltage (0-5V)
VDDA	Power	Analog Power (5 V)
AGND	Ground	Analog Ground
RSL_Sx	Analog In	4x Resolver sense signal Sx (0-12V), 'x'= 1, 2, 3, 4
RSL_Rx	Analog Out	Resolver drive signal Rx (0-12V), 'x'= 1, 2
RSL_DRV_SHD	Ground	Resolver drive signal shield
RSL_SNS_SHD	Ground	Resolver sense signal shield
RTDx_SIG	Analog Out	RTDx resolver signal (0-5V), 'x'= 1, 2
RTDx_RTN	Ground	RTDx resolver sense return, 'x'= 1, 2

4.3 Software architecture

The inverter software architecture, shown in [Figure 6](#), provides a basic foundation for implementing higher level Motor Control Application Software and is comprised of three primary layers:

- Application layer
- Platform API layer (Middleware)
- Abstraction layer

EV Traction Motor Power Inverter Control Reference Platform

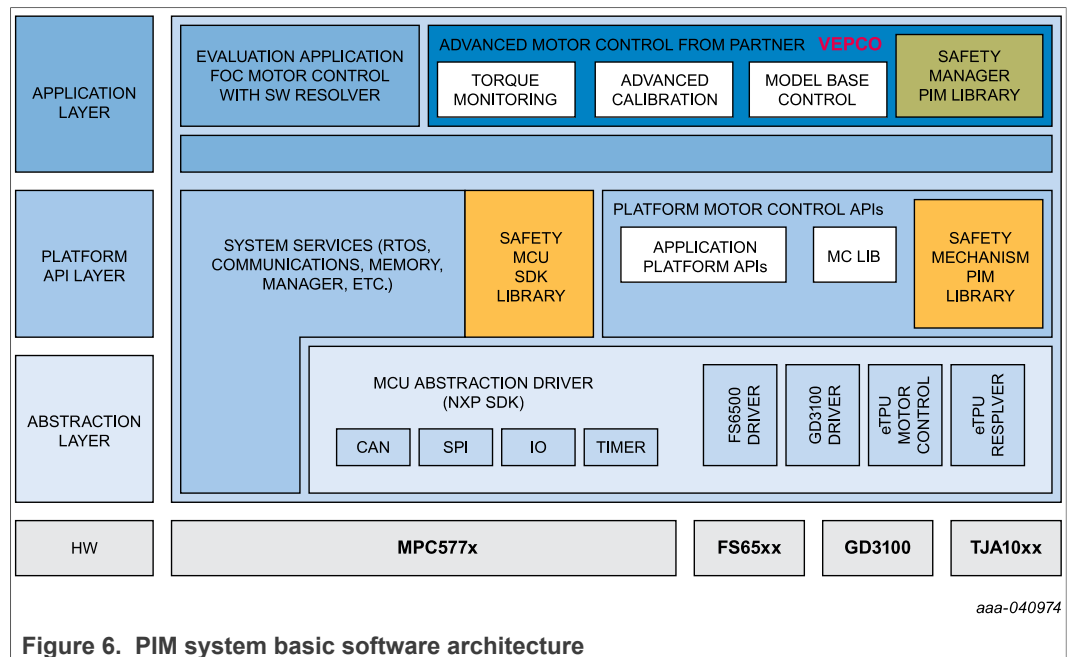


Figure 6. PIM system basic software architecture

4.3.1 Application layer

The Application layer includes a set of function calls run by the Motor Control Application Software³ to control the operation of the inverter platform hardware. Software developer can build their own motor control application software using these APIs.

For a detailed list of application platform API services provided to the application layer, refer to *UM11317 – PIM Software User Manual* (available [here](#) with purchase of the kit) that accompanies the Inverter Control Reference Platform kit.

4.3.2 Platform API layer

The Platform API layer is the Basic Software (BSW) middleware layer which is composed of system service routines, application platform APIs and the motor control library.

System services include the OS services for Periodic task operation and provide services for system operation. The System services also handle the system operating manager component for system state transitions and the Fault manager component for fault management.

Application Platform APIs include the routines for common input and output functions. Common input output functions include all the sensing function APIs to obtain analog sensing for phase currents, bus voltage, and motor temperatures. The platform API layer provides transparency to the application layer to deal with the low-level drivers.

The Motor control library is a library set provided to the application layer for all the motor control and math functions.

For a detailed list of application platform API services provided to the platform API layer, refer to *UM11317 – PIM Software User Manual* (available [here](#) with purchase of the kit).

³ FOC and Motor Control strategy are customer/application dependent and for this specific PIM provided by Vepco.

4.3.3 Abstraction layer

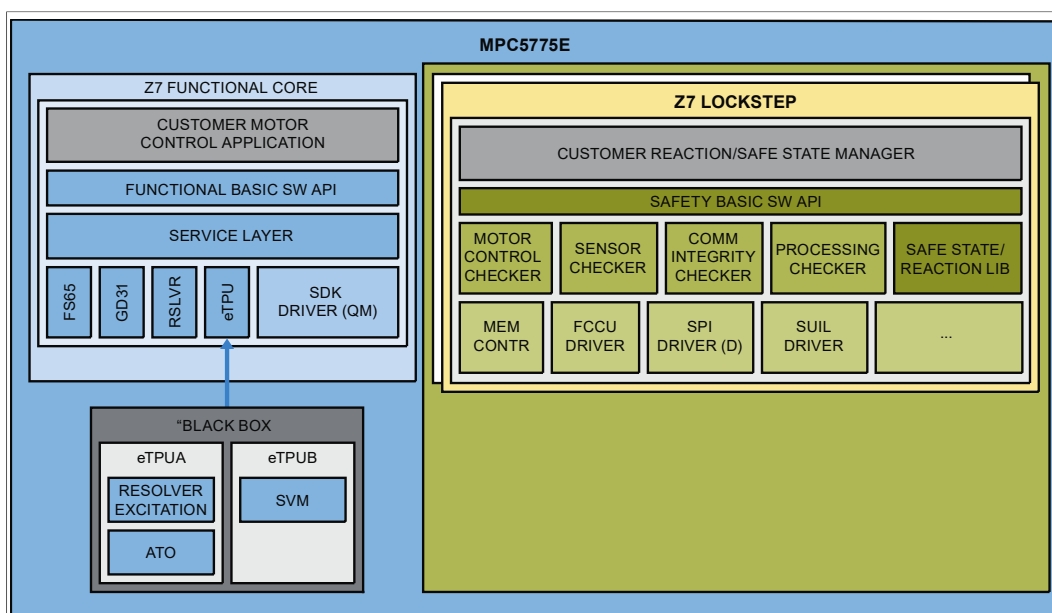
The Abstraction layer abstracts the inverter platform hardware level control of the MCU internal peripherals, the MCU eTPU⁴ timing module for both motor control and resolver functions, the FS65 system basis chip, and the GD3100 IGBT gate driver.

The Abstraction layer consists of MCU low-level software drivers provided from NXP Software development kit (SDK), FS6500 software drivers, GD3100 software drivers, and the eTPU motor control function set ([here](#)).

The software bundle provided with the inverter kit runs with the RTM 3.0.0 SDK update for MPC5775E and the standalone driver for FS6500 and GD3100. The eTPU control set is packaged with the software bundle and can also be downloaded on the eTPU function set link ([here](#)).

The MCU_IO software component provides all the setup for clock initialization, peripheral initialization, and application startup.

The eTPU SW libraries are low-level drivers that have been highly optimized for the MPC577x MCUs. They should be treated as black-box elements.



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Figure 7. Functional and safety software partition

Detailed descriptions of the motor control services functionality can be found in the *UM11317 – PIM Software User Manual* (available [here](#) with purchase of the kit).

4.4 MPC5775E MCU

Key features

On-chip modules available with the MPC5775E include the following features:

⁴ Enhanced Timer Processing Unit (eTPU), a programmable core used to offload CPUs from low-level repetitive tasks

- Three dual issue, 32-bit CPU core complexes (e200z7), two of which run in lockstep
 - Power Architecture embedded specification compliance
 - Instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
 - On the two computational cores: Signal processing extension (SPE1.1) instruction support for digital signal processing (DSP)
 - Single-precision floating point operations
 - On the two computational cores: 16 KB I-Cache and 16 KB D-Cache
 - Hardware cache coherency between cores
- 4 MB on-chip flash memory
- Supports read during program and erase operations, and multiple blocks and EEPROM emulation
- 512 KB on-chip general-purpose SRAM including 64 KB standby RAM
- Two 64 channel multichannel direct memory access controllers (eDMA)
- Dual core Interrupt Controller (INTC)
- Crossbar Switch architecture for concurrent access to peripherals, flash memory, or RAM from multiple bus masters with End-To-End ECC
- Error Injection Module (EIM) and Error Reporting Module (ERM)
- Four protected port output (PPO) pins
- Advanced timers with Programmable cores (Up to three enhanced Time Processor Units (eTPUs))
- Enhanced Modular input/output System (eMIOS) supporting 32 unified channels with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Up to two Enhanced Queued Analog-to-Digital Converter (eQADC) modules with:
 - Two separate analog converters per eQADC module
 - Support for a total of 70 analog input pins, expandable to 182 inputs with off-chip multiplexers
- Up to four independent 16-bit Sigma-Delta ADCs (SDADCs) Ethernet (FEC)
- Two SENT Receiver (SRX) modules supporting 12 channels
- Five Deserial Serial Peripheral Interface (DSPI) modules
- Five Enhanced Serial Communication Interface (eSCI) modules
- Four Controller Area Network (FlexCAN) modules
- Two M_CAN modules that support FD
- Fault Collection and Control Unit (FCCU)
- Clock Monitor Units (CMUs)
- Tamper Detection Module (TDM)
- Cryptographic Services Engine (CSE)
 - Complies with Secure Hardware Extension (SHE) Functional Specification Version 1.1 security functions
 - Includes software selectable enhancement to key usage flag for MAC verification and increase in number of memory slots for security keys
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- On-chip voltage regulator controller (VRC) that derives the core logic supply voltage from the high-voltage supply
- On-chip voltage regulator for flash memory
- Self-test capability

Safety features

- Replication of IP: A dual-core architecture reduces the need for component duplication at the system level and lowers overall system complexity.
- Replication of processing elements: For the dual lockstep z7 cores (Core 1 and Checker) and cache controllers, functional safety is ensured by a lockstep approach. Any deviation in the output of the two lockstep z7 cores is detected by hardware and signaled as a possible failure.
- Error correction or detection to reduce the effect of faults in the following integrated volatile and non-volatile memories:
 - Flash memory
 - SRAM
 - FlexCAN
 - MCAN
 - ENET
 - Cache and cache tags
 - eDMA Transfer Control Descriptor (TCD) RAM
 - eTPU
- Memory Protection Unit (MPU), hardware access control for all memory references generated in the device.
- The generation and distribution of clock and power are supervised by dedicated monitors.
- Built-in self-tests (for example, MBIST and LBIST) are implemented in hardware to detect general latent failures and therefore reducing the risk of coincident failures (multiple-point faults).
- The Fault Collection and Control Unit (FCCU) is responsible for collecting and reacting to failure notifications.
- CMF are dealt with by a set of measures for both control and reduction, spanning system level approaches (such as temperature and non-functional signal monitoring), physical separation, and diversity.
- The functional safety of the periphery is ensured by application level (system level) measures (such as connecting one sensor to different I/O modules, sensor validation by sensor fusion, and so on). For this, the chip ensures that redundant use of peripherals is protected against CMF.
- Usage of internal (and external) watchdogs or timeout measures.
- Dedicated mechanisms are suggested to check the functionality of error reaction paths (such as by application-controlled fault injection).

The MPC5775E safety core operates in delayed lockstep mode (LSM) to allow the highest safety level to be reached. The checker core receives all inputs delayed by two clock cycles. Outputs of the checker core are compared with outputs of the master core.

Any differences are flagged as an error and processed by the FCCU.

The FCCU offers a hardware channel to collect errors and bring the device to a Safe state when a failure is present in the MPC5775E. The FCCU provides two error output signals (ERROR0 and ERROR1) used for external failure indication (i.e. to the SBC⁵).

[Figure 8](#) shows a top-level block diagram of the MPC5775E. The purpose of the block diagram is to illustrate the general interconnection of functional modules through the crossbar switch.

⁵ System Basis Chips: a combination of power supply, communication transceivers and diagnosis features

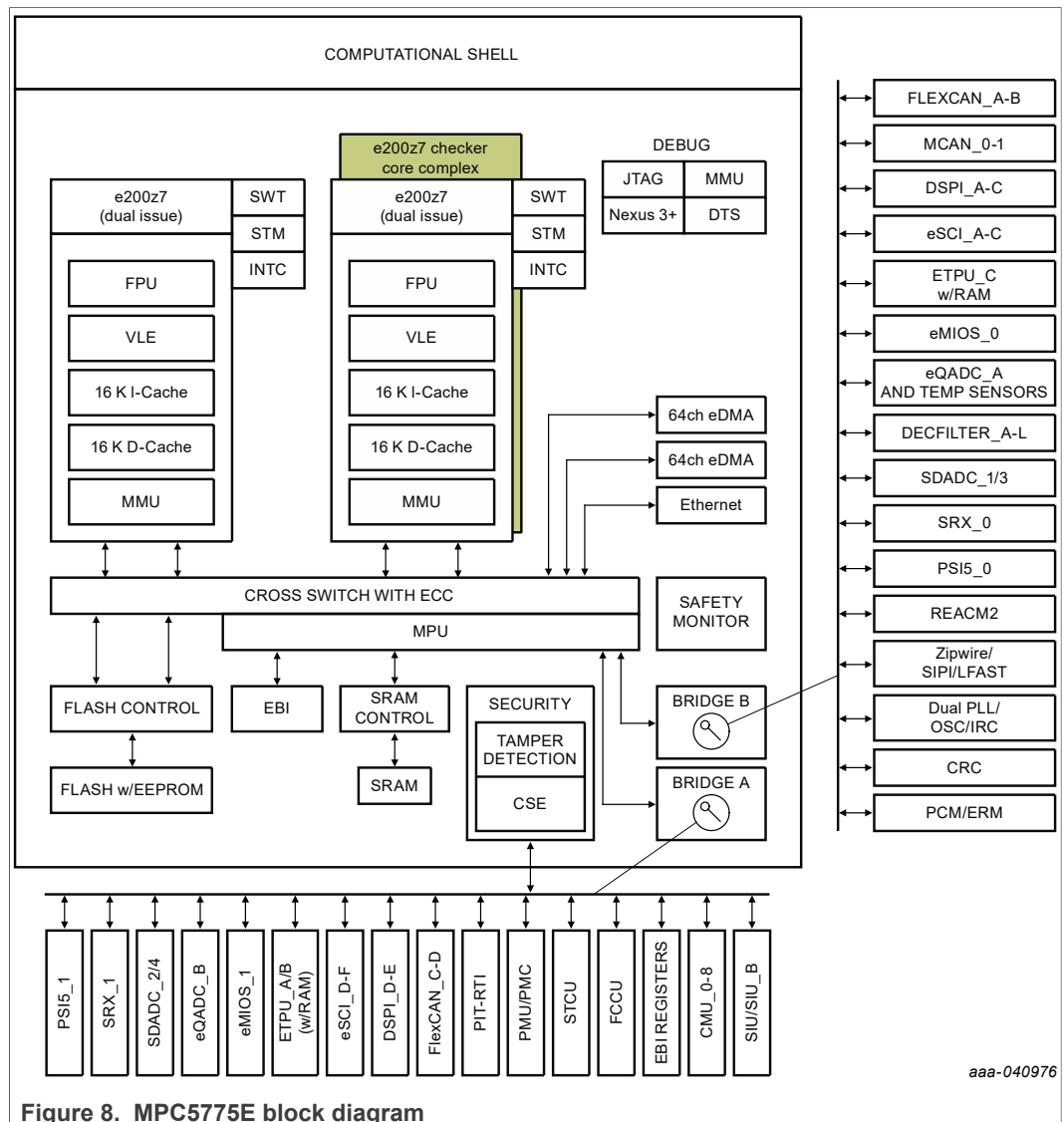


Figure 8. MPC5775E block diagram

For more information, refer to the MPC5775E data sheet and safety manual from NXP ([here](#)).

4.5 FS6523 safe PMIC

The FS6523 SMARTMOS device is a multi-output, power supply integrated circuit that includes CAN Flexible Data (FD) and/or LIN transceivers. The devices are dedicated to the automotive market.

Multiple switching and linear voltage regulators, including low-power mode (32 μ A), are available with various wake-up capabilities. An advanced power management scheme maintains high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS6523 SPMIC includes configurable fail-safe/fail silent safety behavior and features, with two fail-safe outputs. The FS6500/FS4500 SPMIC can be integrated as a full part of a safety-oriented system partitioning. The devices conform to high integrity safety levels (up to ASIL D).

The built-in CAN FD interface fulfills the ISO11898-2 and -5 standards. The LIN interface fulfills LIN protocol specifications 2.0, 2.1, 2.2, and SAEJ2602-2.

Key Features

- Battery voltage sensing & MUX output pin
- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck
- Family of devices to supply MCU core from 1.0 V to 5.0 V, with SMPS (0.8 A, 1.5 A or 2.2 A) or LDO (0.5 A)
- Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (VCCA tracker or independent), 5.0 V or 3.3 V
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (VCCA), 5.0 V or 3.3 V
- 3.3 V keep alive memory supply available in low-power mode
- Long duration timer, counting up to 6 months with 1.0 s resolution
- Multiple wake-up sources in low-power mode: CAN, LIN, I/Os, LDT
- Five configurable I/Os

[Figure 9](#) shows a block diagram of the FS6523

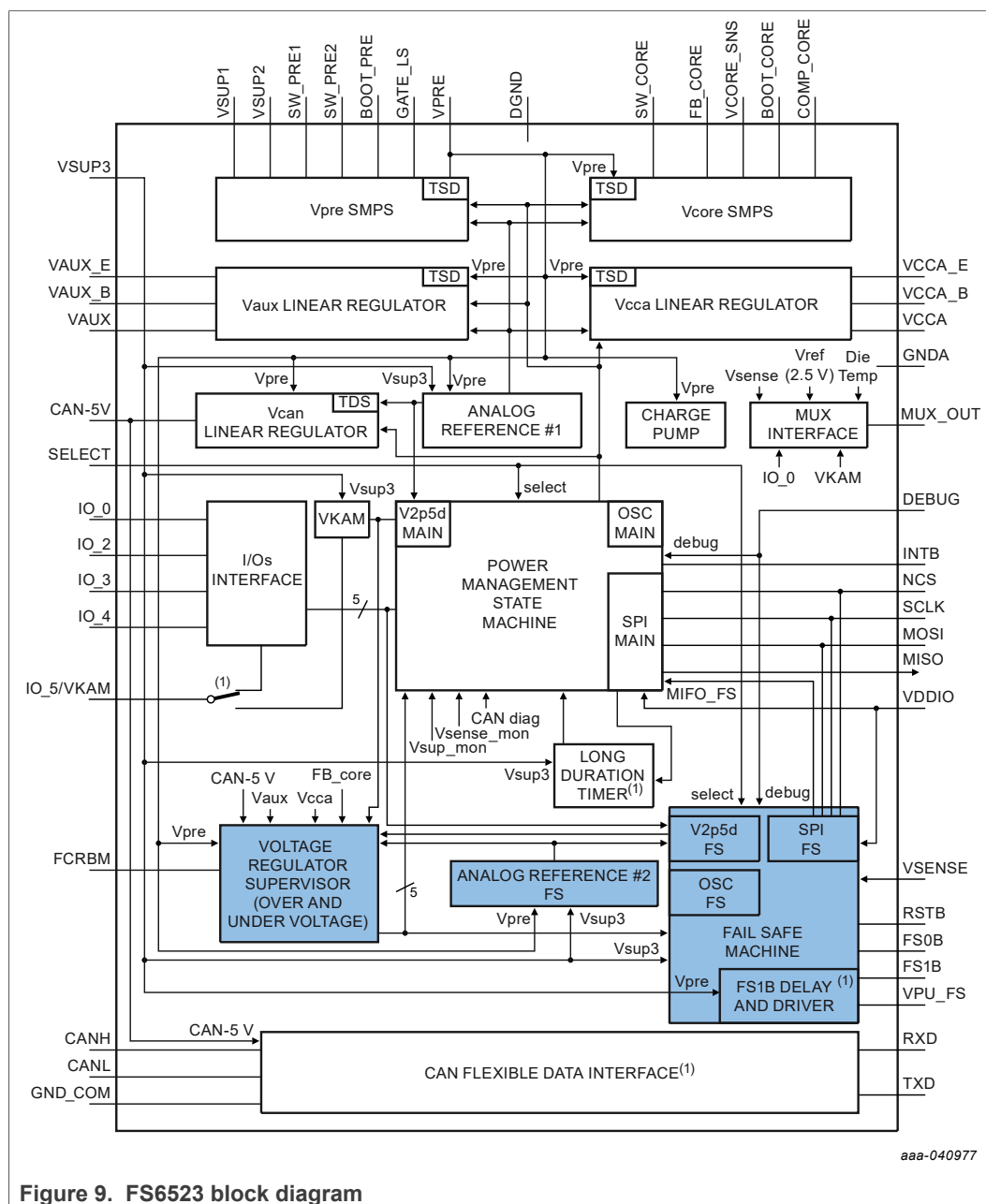


Figure 9. FS6523 block diagram

For more information, refer to the FS6523 data sheet from NXP ([here](#)).

4.6 MC33GD3100 isolated high-voltage IGBT gate driver

The MC33GD3100 is an advanced single channel gate driver for IGBTs and SiC power devices. Integrated Galvanic isolation and low on-resistance drive transistors provide high charging and discharging current, low dynamic saturation voltage, and rail-to-rail gate voltage control.

Current and temperature sense minimizes IGBT stress during faults. Accurate and configurable under voltage lockout (UVLO) provides protection while ensuring sufficient gate drive voltage headroom.

The MC33GD3100 autonomously manages severe faults and reports faults and status via the INTB pin and an SPI interface. It is capable of directly driving gates on most IGBTs and SiC MOSFETs. Self-test, control, and protection functions are included for design of high reliability systems (ASIL C/D). The device meets the stringent requirements of automotive applications and is fully AEC-Q100 grade 1 qualified.

Key features

- SPI interface for safety monitoring, programmability and flexibility
- Low propagation delay and minimal PWM distortion
- Integrated Galvanic signal isolation (up to 8 kV)
- Integrated gate drive power stage capable of 15 A peak source and sink
- Fully programmable Active Miller Clamp
- Compatible with negative gate supply
- Compatible with current sense and temperature sense IGBTs
- Integrated soft shutdown, two-level turn-off, active clamp, and segmented drive for wave shaping
- CMTI > 100 V/ns
- Compatible with 200 V to 1700 V IGBT/SiC, power range > 125 kW
- Operating temperature range -40 °C to 125 °C
- External Creepage distance (CPG): > 7.8 mm
- Operating frequency > 40 kHz
- 5.0 V and 3.3 V tolerant MCU interface available

Safety features

- Certified to ASIL D ISO26262 functional safety requirements for full diagnostics
- Current, DESAT, and temperature sense inputs and ADC reporting for IGBT/SiC monitoring
- Fast short-circuit protection, overcurrent protection, temperature warning, and shutdown
- Interrupt pin for fast response to faults
- Built-in self-check of all analog and digital circuits
- Continuous watchdog of die-to-die communications
- Deadtime enforcement
- Over and undervoltage supervision of all power supplies on both low and high-voltage sides
- Fail-safe state management pins on both low and high-voltage sides
- VGE real time cycle-by-cycle monitoring

Safety and regulatory approvals

- Reinforced Isolation per DIN V VDE V 0884-10
- Withstands 5000 V rms (1 minute) isolation per UL 1577
- CSA Component Acceptance Notice 5A
- AEC-Q100 grade 1 automotive qualified

[Figure 10](#) shows a block diagram of the MC33GD3100

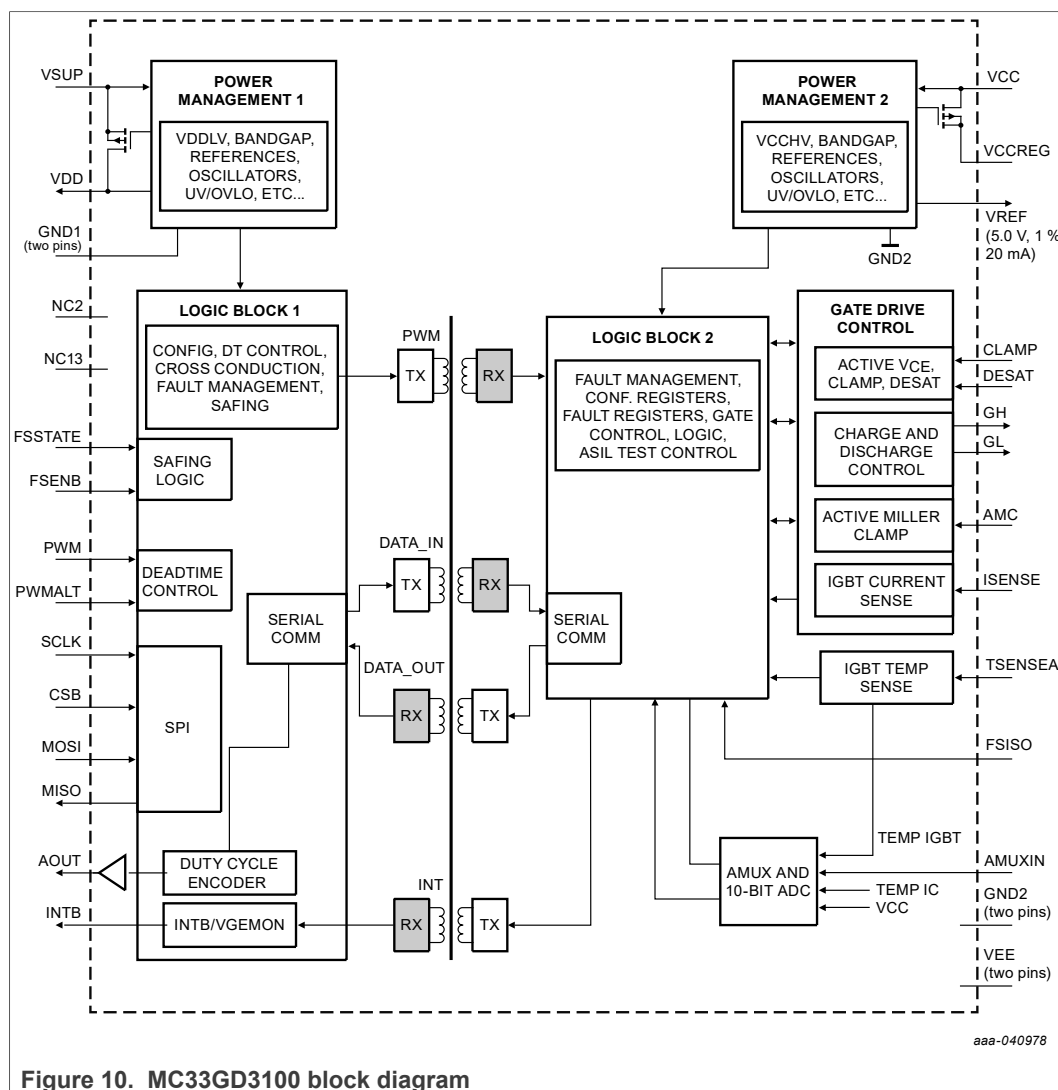


Figure 10. MC33GD3100 block diagram

For more information, refer to the MC33GD3100 data sheet from NXP ([here](#)).

4.7 TJA1051T/3 high-speed CAN transceiver

The TJA1051 is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing a differential transmit and receive capability to an MCU with a CAN protocol controller.

The TJA1051 belongs to the third generation of high-speed CAN transceivers from NXP Semiconductors, offering significant improvements over first- and second-generation devices such as the TJA1050. It offers improved Electromagnetic Compatibility (EMC) and Electrostatic Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- A very low-current Standby mode with bus wake-up capability
- The ability to interface directly to microcontrollers with supply voltages from 3 V to 5 V

The TJA1042 implements the CAN physical layer as defined in the current ISO11898 standard (ISO11898-2:2003, ISO11898-5:2007) and the pending updated version of ISO 11898-2:2016. Pending the release of the updated version of ISO11898-2:2016 including CAN FD and SAE J2284-4/5, additional timing parameters defining loop delay symmetry are specified. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s.

These features make the TJA1051 an excellent choice for all types of HS-CAN networks in nodes that do not require a standby mode with wake-up capability via the bus.

Key general features

- Fully ISO 11898-2:2003 compliant
- Timing guaranteed for data rates up to 5 Mbit/s in the CAN FD fast phase
- Suitable for 12 V and 24 V systems
- Low Electro Magnetic Emission (EME) and high Electro Magnetic Immunity (EMI)
- VIO input allows for direct interfacing with 3 V to 5 V microcontrollers
- Available in SO8 package and leadless HVSON8 package (3.0 mm # 3.0 mm) with improved Automated Optical Inspection (AOI) capability
- Dark green product (halogen free and Restriction of Hazardous Substances (RoHS) compliant)
- AEC-Q100 qualified

Predictable and fail-safe behavior features

- Functional behavior predictable under all supply conditions
- Transceiver disengages from the bus when not powered up (zero load)

Protection features

- High ESD handling capability on the bus pins
- Bus pins protected against transients in automotive environments
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on pins VCC and VIO
- Thermally protected

For more information, refer to the TJA1051 data sheet from NXP ([here](#)).

5 Functional Operation

The Power Inverter Control Reference Platform has been optimized to offer the maximum efficiency and the maximum safety standard with an efficient Bill of Material (BOM).

The Platform has been implemented and validated on a Proof-of-Concept 150kVA HW Power Inverter Prototype build in collaboration with Vepco (<http://www.vepcotech.com>).

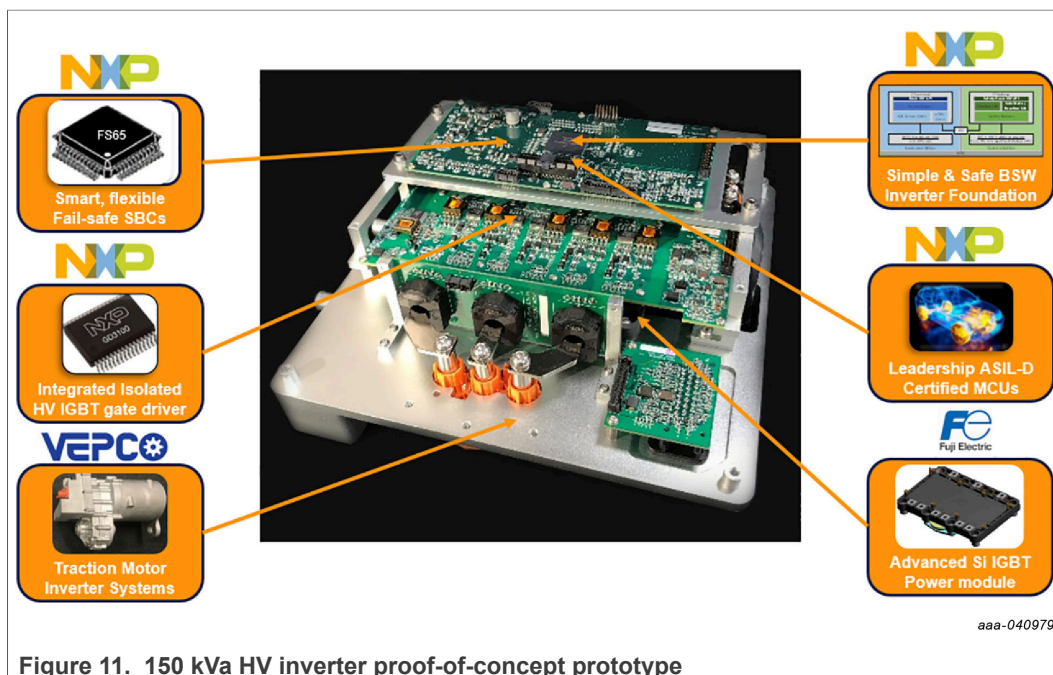


Figure 11. 150 kVa HV inverter proof-of-concept prototype

In general, the output power level of the motor must be in the order of 100-150 kW and the primary function of the Power Inverter Control Reference Platform—referred to hereafter by the generic term Power Inverter Module (PIM)—is to provide different control strategies for the traction motor of a EV/HEV vehicle.

The main function of the unit is to convert a DC power input, which is typically from a high-voltage battery, into a three-phase AC power output capable of driving a motor and precisely controlling the torque output of the motor via the implementation of the closed loop feedback control strategy.

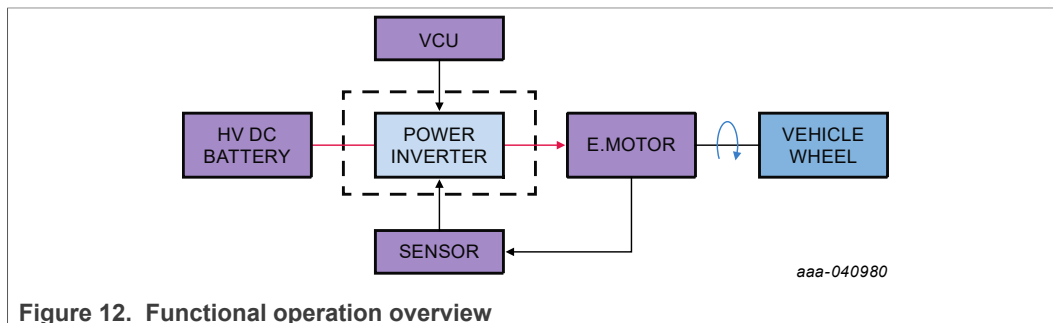


Figure 12. Functional operation overview

A typical operating condition can be described as follows: When the driver starts the electric vehicle, the PIM powers up in Startup Mode and executes system initialization and some safety self-checks. If no fault occurs during Startup Mode, the PIM next enters Normal Mode. At this point, the PIM is ready to interpret commands from CAN bus and the motor is ready to output torque to the wheels as per the driver's command. The PIM

then continuously drives the motor according to the commands received from the VCU. When the PIM detects system faults or any partial failures, it enters a degraded mode and proceeds to a safe state to prevent any hazardous events from occurring. Finally, when the vehicle is powered off, the PIM enters Shutdown mode.

5.1 System control flow

From a functional point of view, as illustrated in Figure 13, the PIM can be logically divided into four subsystems:

- Vehicle Control Unit (VCU) Interface
- MCU and SW Control
- PWM Signal to Power Delivery
- Sensor Feedback

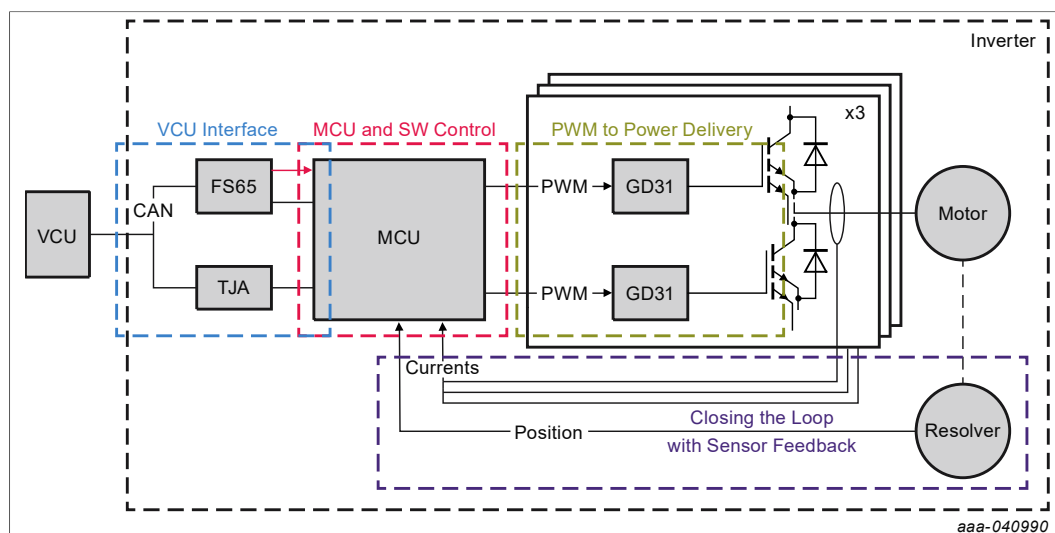


Figure 13. PIM subsystems

5.1.1 VCU interface

The ignition signal is provided by the VCU to this interface for power-up. The VCU interface provides two paths of communication with the VCU. This provides redundancy to the VCU control for functional safety purposes and also guarantees the integrity of the communication.

- FS65 CAN interface
- TJA1051 CAN Interface

The VCU Interface consists of FS65 functions that include power for all the sensors, drivers, MPC5775E, and communication. The VCU Interface also allows the system to be brought into the safe state. It can also act like latch on/latch off system, if required.

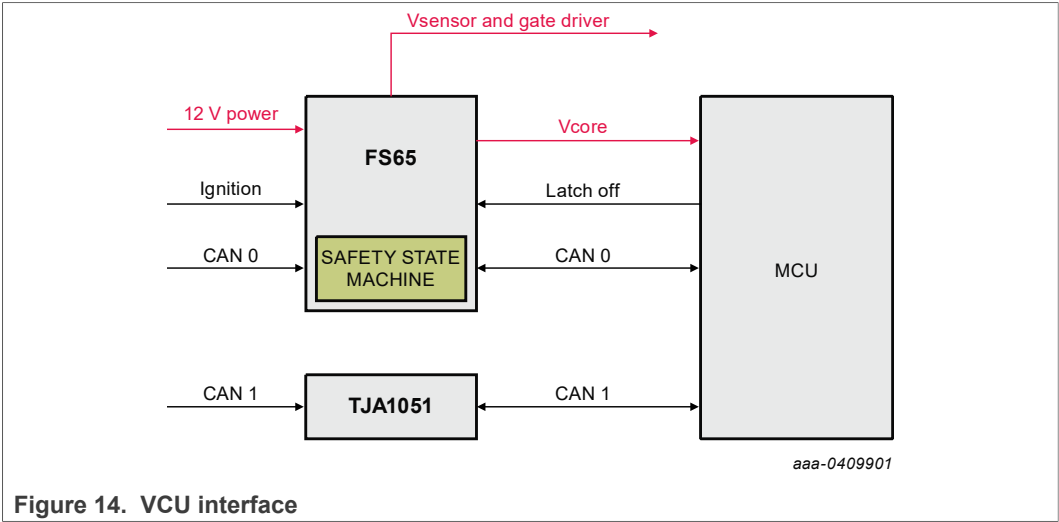


Figure 14. VCU interface

5.1.2 MCU and software control

With the CPU as the heart of the system, MPC5775E runs the FOC motor control software by providing some key benefits to the design. The MCU can be configured in different topologies for different use cases. One such topology, shown in [Figure 15](#) is used in the inverter kit to off-load main motor control tasks from the CPU. [Figure 15](#) shows module interconnections for a typical PMSM FOC application working in sensor-based mode using eTPU Motor Control Library functions involvement.

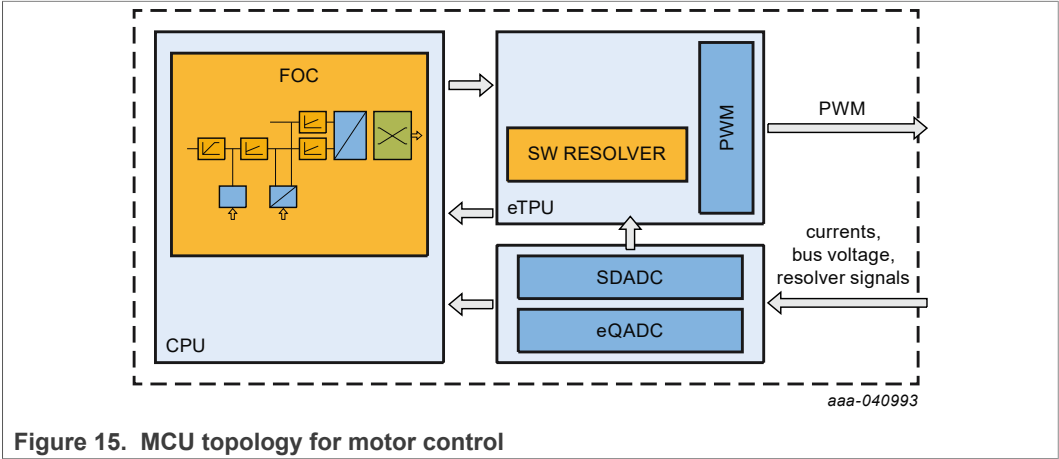


Figure 15. MCU topology for motor control

The key module for motor control on the MPC5775E device is the Enhanced Time Processing Unit (eTPU). Using the eTPU Motor Control library function set, this programmable timer co-processor is capable of generating 3-phase PWM complementary output, analog signal measurement triggering, and synchronization signals, as well as Resolver feedback signal processing.

Using the eTPU to emulate PWM peripheral and SD ADC for resolver processing while running the control algorithm on the CPU, the core is partially off-loaded from the motor control task and can perform higher control loop and switching frequencies.

5.1.3 eTPU

The Enhanced Time Processing Unit (eTPU) is a programmable I/O controller with its own core and memory system, allowing it to perform complex timing and I/O management independent of the CPU. The eTPU is used as a co-processor specialized for advanced timing functions, such as handling complex engine control, motor control, and communication tasks independent of the CPU.

A new complex library of eTPU functions enabling the eTPU to drive motor control applications was developed. This library represents a step forward compared to its predecessor – the motor control function sets (set3 and set4).

The MCU, apart from the PMSM FOC control, manages the Inverter and the system control of FS6500 and GD3100 to achieve a system safe state. This is accomplished by safe state logical connections among the FS6500, the MPC5775E, and the GD3100.

5.1.4 MPC5775E integrated with FS6500

Integrating FS6500 with the MCU provides safety monitoring capabilities for the inverter system. [Figure 16](#) shows how the safety monitoring works.

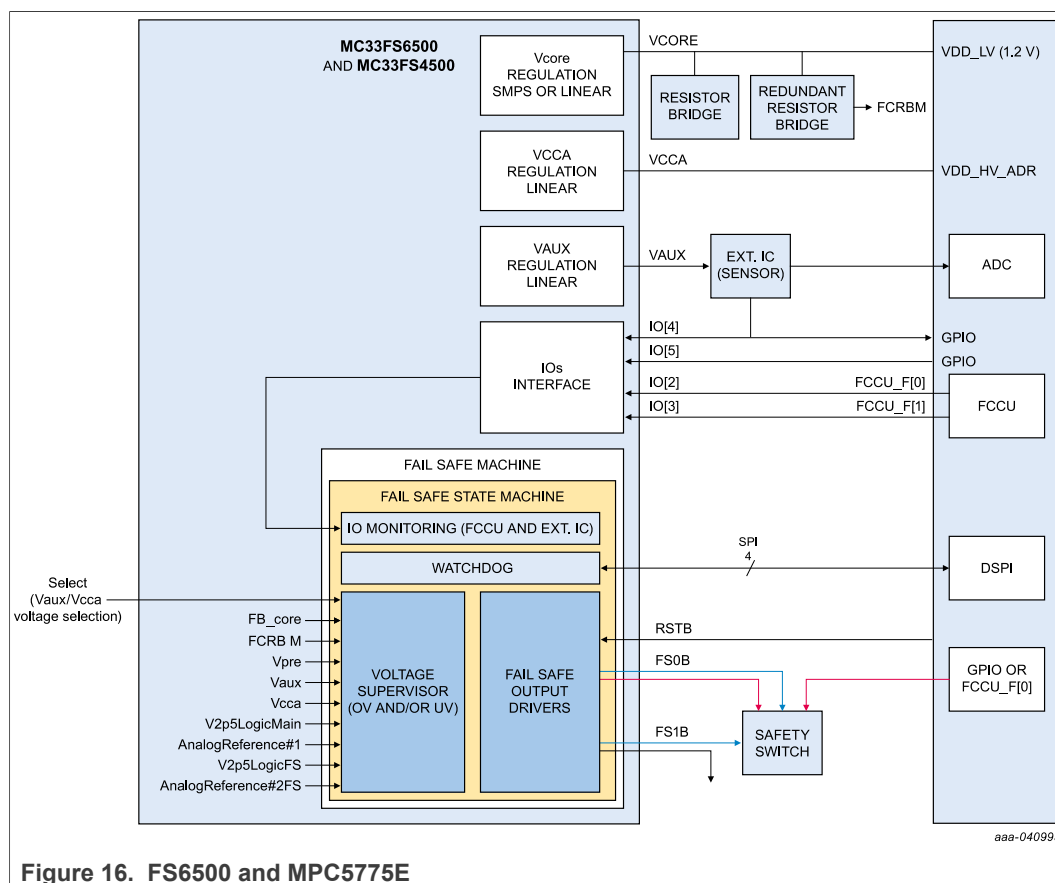


Figure 16. FS6500 and MPC5775E

MCU Monitoring: FS6500 IO_2:3 can monitor the Fault collection control unit (FCCU) pins from MPC5775E.

Redundancy monitoring: FS6500 IO_4:5 can monitor the error output pin from the external IC in redundancy with the MPC5775E.

Redundant safety pin (FS0b): FS0b provides a redundant system fail-safe path for a high level of functional safety. A second Fail-safe pin(FS1B) provides a means of asserting a safety path with configurable delay after failure.

5.1.5 MPC5775E integrated with GD3100

Integrating the GD3100 with the MCU provides PWM updates to the GD3100 and safe monitoring capabilities for the inverter system. [Figure 17](#) shows how the control and the safety monitoring works.

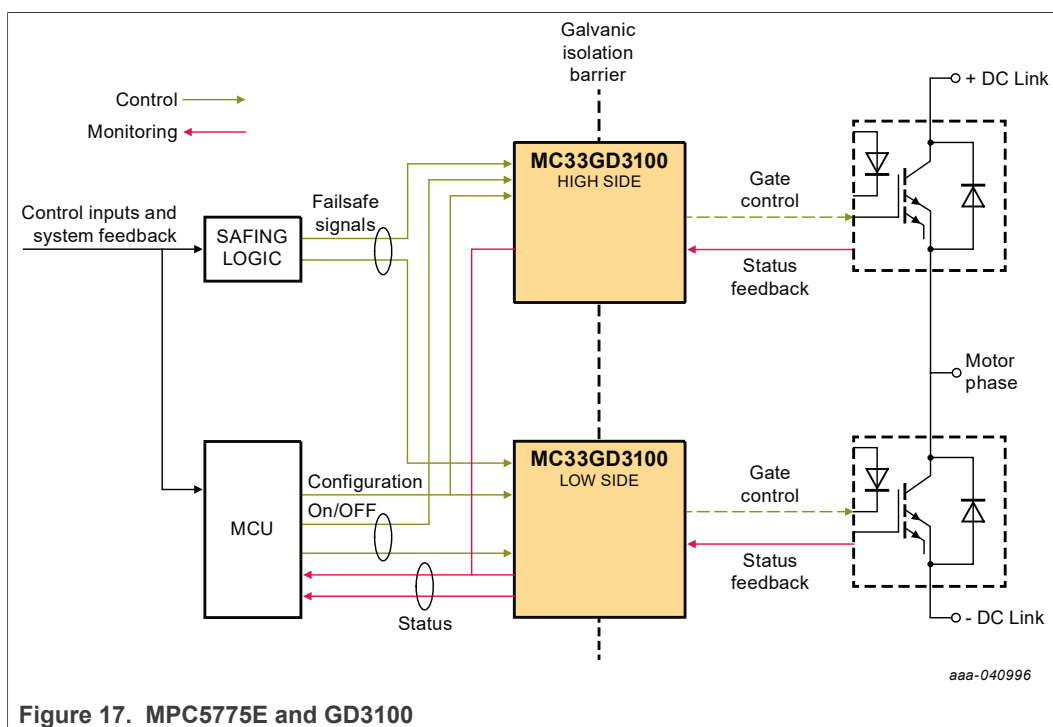


Figure 17. MPC5775E and GD3100

Excitation of power FETs is ensured by GD3100. This analog device ensures external FETs drive at power supply voltages.

Configuration of the GD3100 is realized via the SPI module. The GD3100 allows different operating modes to be set and locked by SPI commands. SPI commands also report the condition of the GD3100 based on the internal monitoring circuits and fault detection logic. The MPC5775E detects gate driver fault states by means of fault signal GD3100 pins.

5.2 Software resolver

The PIM system implements a software interface to the resolver. The resolver software is executed on a dedicated timer core (eTPU) so that the main cores can be focused on higher level tasks. Using a software-based resolver external hardware interface between the motor resolver and MCU ADCs is not needed because the processing is done in software within the MCU using eTPU.

The Resolver Digital Interface eTPU function (RESOLVER) uses one eTPU channel to generate a 50% duty-cycle PWM output signal to be passed through an external low-pass filter and used as a resolver excitation signal. In the resolver position sensor, this excitation signal is modulated by the sine and cosine of the actual motor angle. The feedback Sine and Cosine signals are sampled by an on-chip ADC and the conversion

results can be transferred to eTPU DATA RAM by eDMA. Then, the eTPU function RESOLVER processes the digital samples of the resolver output signals. Motor angular position, angular speed, a revolution counter, and diagnostics are results of the Sine and Cosine feedback signal processing.

For more information about eTPU Resolver implementation and its configuration, refer to eTPU RDC and RDC Checker User Guide ([here](#)).

In particular, the SW resolver processes the resolver outputs (sin/cos) with the help of SD-ADC, and calculates by using application dedicated cores:

- Angular position
- Angular speed
- Resolver excitation
- Diagnosis

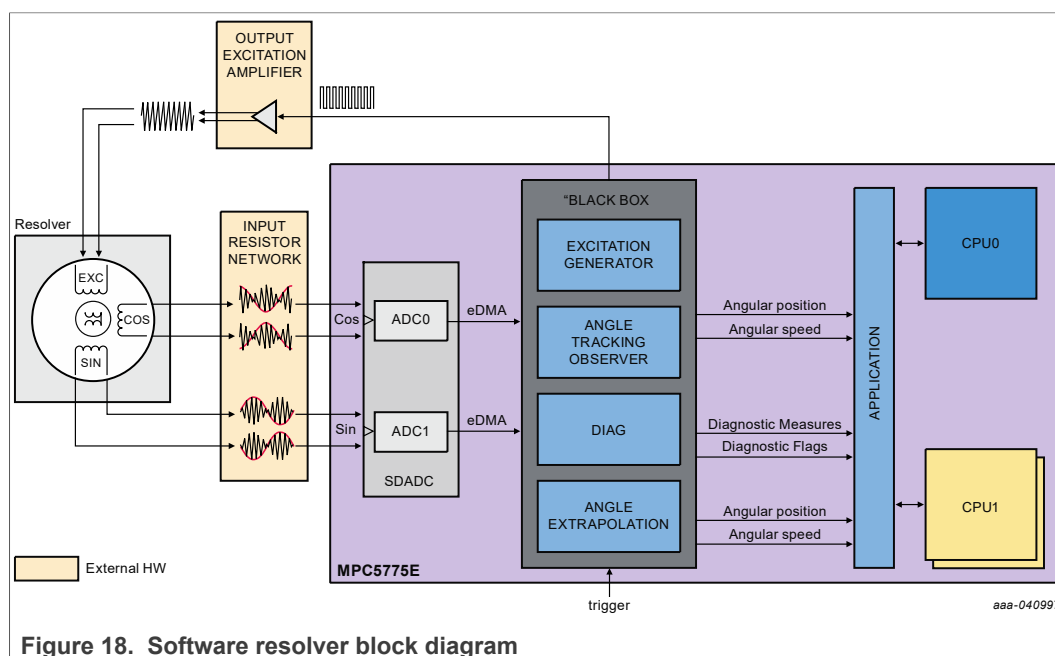


Figure 18. Software resolver block diagram

From the Application layer point of view, the SW resolver functionality is considered as an HW module.

6 Safety Concept Overview

6.1 Introduction

This section presents an overview of a system safety concept for a high-voltage traction inverter for an electric vehicle. To facilitate the design of a functionally safe EV/HEV vehicle, this section provides an example of a safety concept based on NXP components for a traction Inverter.

For additional information on Part 3 and Part 4 of the ISO26262 process, see the following application notes: *Functional Safety Concept of High-Voltage Traction Inverter* ([here](#)) and *NXP System Safety Solution: High Voltage Traction Inverter* ([here](#)).

6.2 Safety context of a traction inverter

A traction inverter is the main traction system of an electric vehicle. It accelerates the main traction motor and provides regenerative braking according to the torque request from a Vehicle Control Unit ([Figure 19](#) and [Figure 20](#)).

For battery electric vehicles, the motor is generally attached directly to the wheel with a simple gearbox with a 8:1 to 10:1 Ratio. The main safety hazards for this type of system are unintended traction, unintended braking, and HV electrocution. Such concerns are addressed differently by car manufacturers and their ASIL ratings vary between ASIL-B to ASIL-D.

In this analysis, the safety goals are:

- **SG1:** Avoid Over accelerating torque beyond 50 Nm or +5% of the requested torque (ASIL-D, FTTI=200 ms)
- **SG2:** Avoid Over Braking torque beyond 50 Nm or +5% of the requested torque (ASIL-D, FTTI=200 ms)

[Figure 19](#) and [Figure 20](#) show a typical traction inverter system.

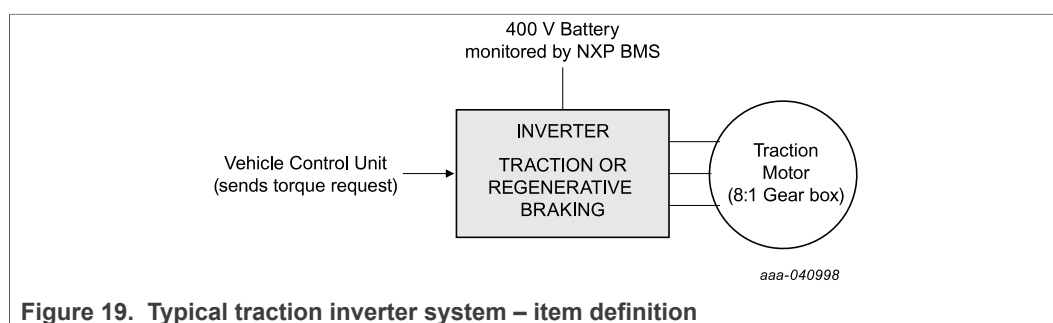


Figure 19. Typical traction inverter system – item definition

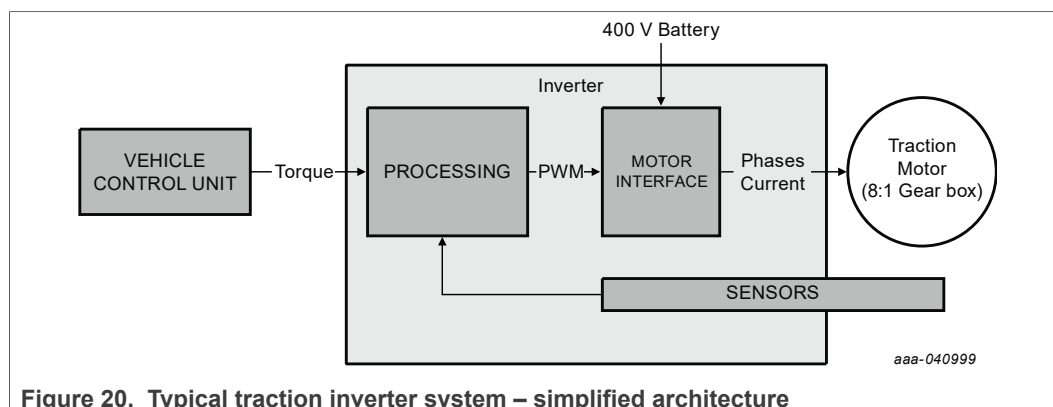


Figure 20. Typical traction inverter system – simplified architecture

The typical traction inverter system control flow is:

- A torque command is sent from a VCU to the Inverter through CAN.
- This torque command is received by the Processing Unit.
- The Processing Unit computes the next PWM duty cycle according to the command and the state of the system.
- The motor interface turns on/off the motor phases according to the received PWM.
- The Processing unit measures the state of the system (current, position, speed, voltage) to close the loop and correct the error.

This simplified architecture explains the safety concept of the NXP traction solution. For a more detailed explanation of the ISO26262 methodology (from the Safety goals, to the functional, technical and hardware and software requirements), see the safety package offered by NXP.

6.3 Doer – Checker processing architecture

In the Processing domain, communication failures and computation failures represent the most likely violations of Safety Goal SG1 and SG2. Communication failures are not addressed in this document. The safety mechanism for such systems are usually standard integrity checkers in the CAN command to guarantee the integrity of the received command and the availability of the sender and receiver.

The architecture used to prevent computation failure for this system is a Doer–Checker architecture (Figure 23). The Doer implements the main functional requirements with complex algorithms such as field-oriented control, advanced control techniques, and math functionality. The checker detects unsafe situations and brings the system into a safety state. This allocation reduces the complexity in the safety system because all the safety requirements are allocated to the Checker while the Doer focuses on system performances. In ISO26262 vocabulary, this means that the safety requirements allocated to the Doer are QM (Quality Managed) while the safety requirements allocated to the Checker are ASIL-D. In this study, the Checker functions and requirements are grouped into a system module called the Safety Manager.

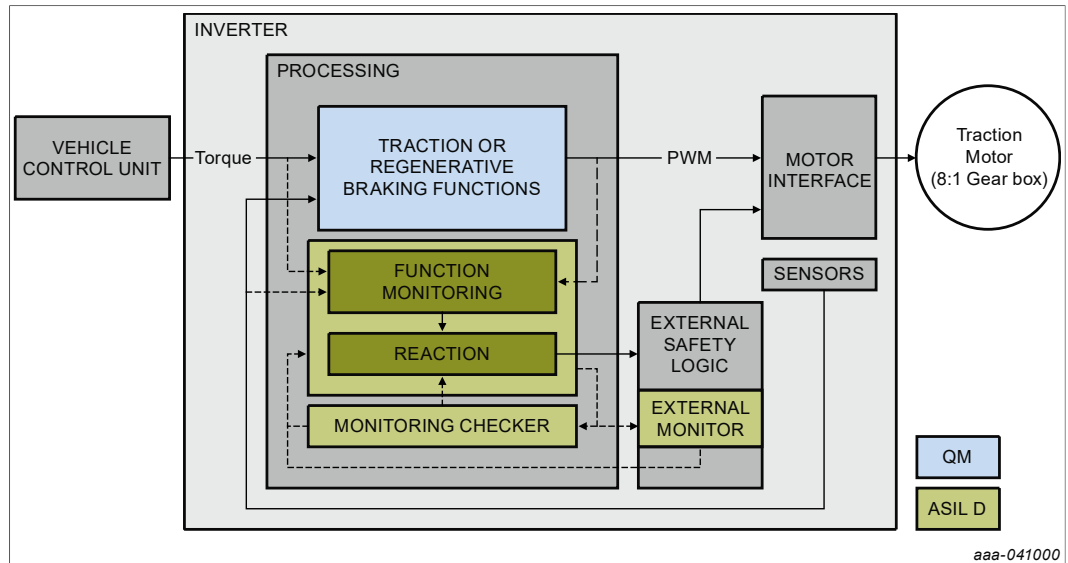


Figure 21. Safety allocation processing

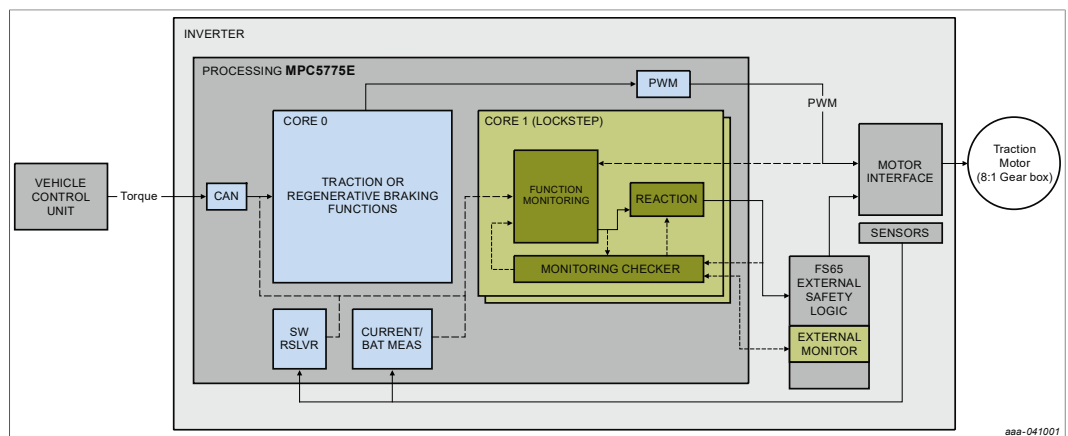


Figure 22. Allocation of functions in the MPC5775E cores

The Safety Runtime Framework for Power Inverter is a flexible modular library of functions that allow customers to implement the Safety Manager requirements according to the NXP Safety Runtime Framework.

6.4 Motor interface safety concept for a permanent magnet motor

One constraint in the new generation of electric vehicles is the high Back Electro-Magnetic Field (BEMF) generated by the permanent magnet synchronous motor. At high speed, when PMSM's phases are left open ([Figure 23](#)), the generated BEMF voltage can be higher than the battery voltage, which causes a regenerative current and an unintended braking torque on the vehicle. To prevent this hazard, the system must react by shorting the high side (3-Phase Short High side 3PSHS) ([Figure 24](#)) or the low side (3-Phases Short Low Side 3PSLS) ([Figure 25](#)) of the half bridges (safe state).

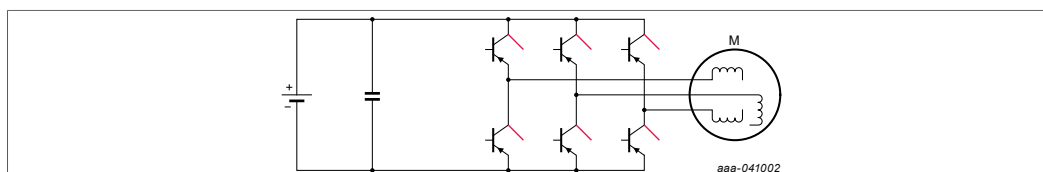


Figure 23. 3-phase Open (unsafe at high speed)

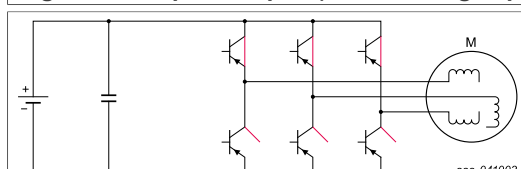


Figure 24. 3-phase Short High-Side

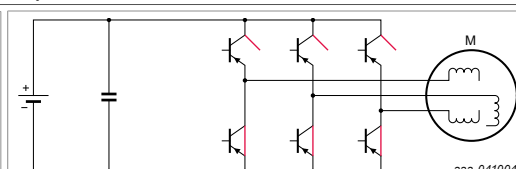


Figure 25. 3-phase Short Low-Side

These applications specific requirements translate into the following architecture:

- **An independent architecture of the high-side and low-side driver bridge control:** if a single point failure makes both the high side and the low side unavailable, the system is not able to react appropriately.
- **Quick Short circuit protection (Figure 23):** A short circuit could permanently damage the entire bridge, putting the system into an unsafe state. Such failures are too fast to be handled by the MCU. Therefore, the GD3100 must detect and prevent short circuits.
- **High level of diagnostics for appropriate reaction (Figure 24):** Motor interface failures can occur in a number of different areas (motor phases, IGBT, gate driver, discrete components, cooling). Each may require a different reaction to bring the system back into a safe state. A high side short failure requires the three phases shorted to battery (3PSHS), while a high open failure requires the three phases shorted to ground (3PSLS) at high speed. The GD3100 is designed to have a high level of diagnostics in accordance with the ASIL-D process and to detect 99% of its own faults, as well as other system failures (motor and IGBT) and to report faults to the MCU-Safety manager through a redundant interface.
- **Reaction channel (Figure 25):** Once a fault is reported, the MCU-Safety manager decides which safe state is the most appropriate. A redundant GD3100 channel allows control of the safety state through a dedicated pin. The decision and reaction must be taken within the FTTI ~100 μ s.

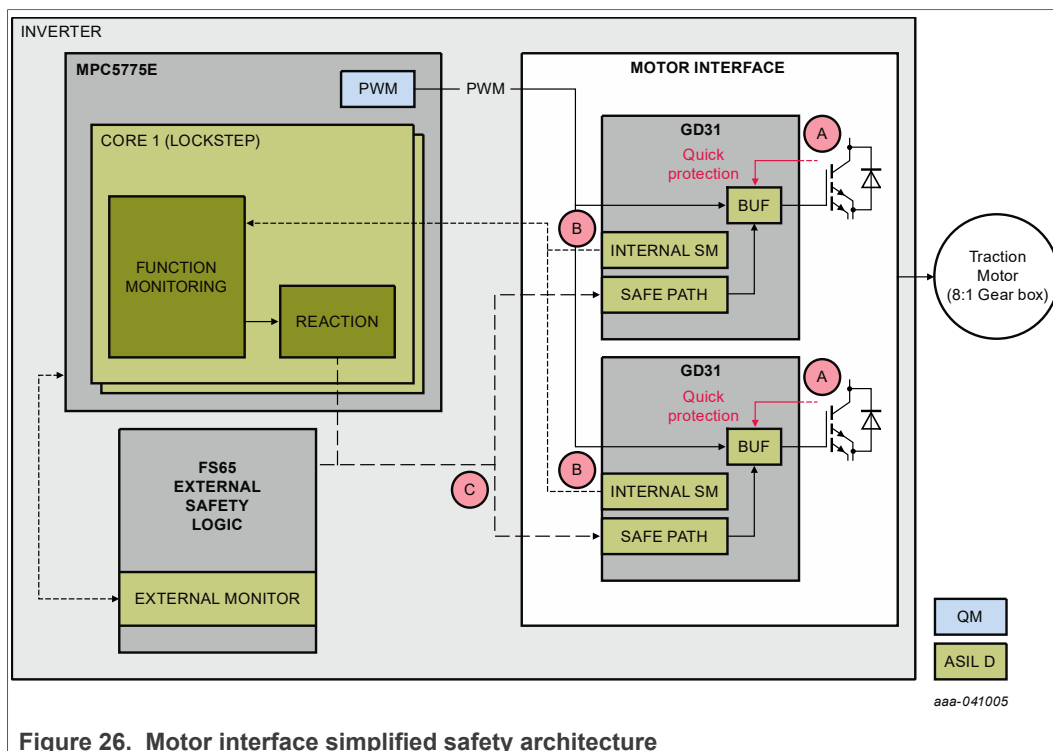


Figure 26. Motor interface simplified safety architecture

The NXP gate driver GD3100 is a key part of this architecture and offers the following advantages over competitive devices:

- Direct control of the IGBT/SiC without a booster, which allows a reduction of the overall failure rate and direct control of the safety path through the gate driver
- Quick short circuit protection (<2 μ s for IGBT, faster for SiC) with turn-off wave-shaping management to avoid destructive overshoots (SSD 2LTO)
- High diagnostic coverage: The GD3100 is designed specifically for an automotive ISO26262 process. The device's diagnostic features include high diagnostic coverage for internal faults, Built-In Self Test (BIST) functionality, a Watchdog timer, and CRC capabilities

6.5 Communication and sensors safety concept

To close the loop, the motor control algorithm uses the phases' current, the motor angle position, and the battery voltage. A wrong sensor acquisition has a direct impact on the command applied to the motor. Safety requirements for sensors entail the ability to diagnose any failure in the acquisition chain (the sensors, amplification, analog to digital conversion, and sensor data pre-processing). This document focuses only on the motor position as an example. The methodology is similar for the current and battery voltage.

The system uses a mechanical resolver mounted on the shaft of the motor, an amplification chain, and a software resolver (eTPU). The eTPU uses a combination of processor and timer channels to process complex timing events. The advantage of this architecture is that it avoids computing cycle consumption on Core 0.

The flow chain is represented in blue in [Figure 27](#):

- The eTPU creates an excitation signal to excite the primary of coil.
- Two coils 90 degrees shifted measure the sin and the cos of this signal. The received excitation varies depending on the shaft angle.

- Sigma delta ADCs measure the two signals, synchronously of the excitation signal. The results are put in the eTPU RAM for processing.
- The signal is demodulated, and the angle and speed are calculated using a tracking observer model. To improve the accuracy the angle is extrapolated to correct the error due to the delay between the acquisition time to the end of processing time.
- The angle is consumed by the motor control algorithm.

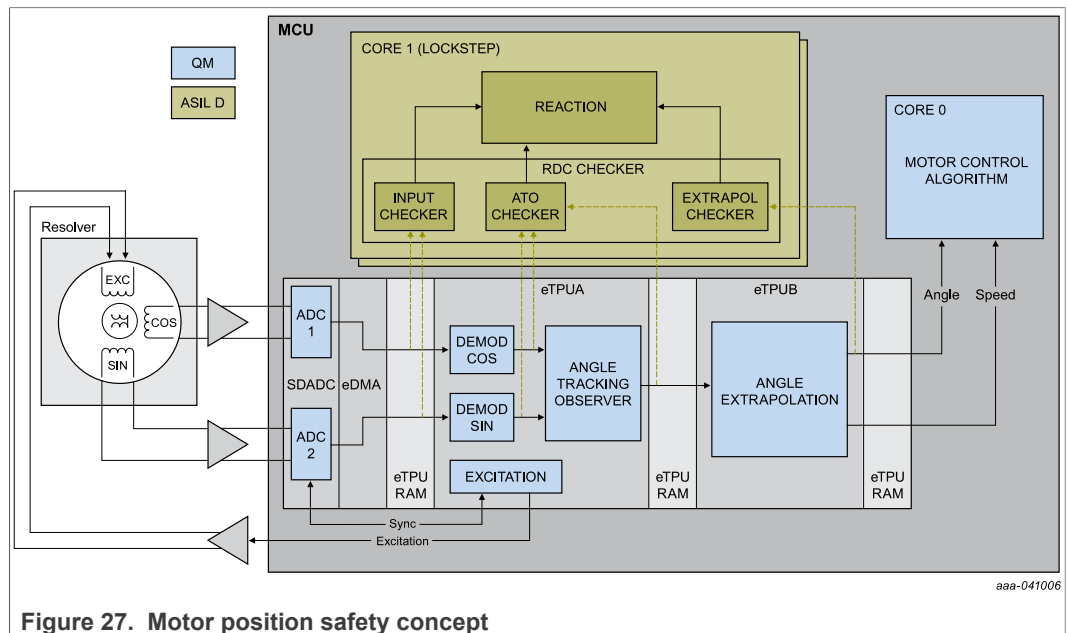


Figure 27. Motor position safety concept

The RDC Checker library inputs data to the safety core and performs diagnostics that are passed to the flows chains to diagnose all possible faults.

The input checker looks at the raw values to calculate the synchronization of the excitation signal with zero crossing, the maximum and minimum amplitude, and the unit vector. It detects 99% of hardware failures of the amplification, coils, excitation chains, SD-ADC.

The ATO Checker computes the angles differently from the eTPU tracking model and runs some plausibility checks. It detects failure of the ETPU computation. Similarly, the extrapolation Checker implements safety mechanisms to detect failures of the angle extrapolation functions.

The RDC Checker (as well as the motor interface, MCU LL safety, etc.) are part of the NXP Safety Inverter Library that is distributed with the hardware solution. It is a flexible, modular library that allows customers to adapt NXP assumptions to their own safety case.

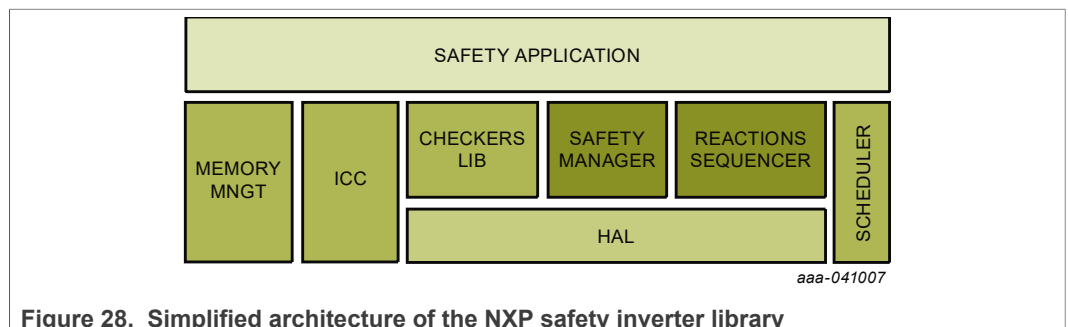


Figure 28. Simplified architecture of the NXP safety inverter library

6.6 Deliverables of the safety enablement

The processing, the motor interface, and the motor position safety concepts are three simplified examples of NXP safety architecture for EV traction systems. More detailed descriptions, including traceable requirements, ASIL allocation and decomposition, state machines, and failure analysis are available in the FSC (Functional Safety Concept) and TSC (Technical Safety Concept) applications notes delivered under NDA to customers. These concepts are made to be flexible and adaptable by customers to their own applications. They were implemented in hardware and software as part of the NXP EV Power Inverter Reference Platform ([here](#)).

In addition, to simplify the usage of the complex hardware, software, and system safety mechanism, NXP also offers an application specific library to accelerate customer safety development. Contact the NXP Sales representatives for more information.

7 General Electrical Characteristics

TA = -40 °C to 125 °C, unless otherwise specified. VSLV range from FS65 VSUP_UV_L specification up to 36 V, unless otherwise specified. All voltages are referenced to ground.

Table 3. Electrical characteristics

Symbol	Parameter	Value	Unit	Notes
VSLV	Primary low-voltage power supply	12 (4.5-18)	V	Low range limited by LDO selection; high range extendable to 36 V with flyback converter design adjustment
I _{VSLV_PWM_ON}	VSLV operating current (PWM switching)	1.2	A	
I _{VSLV_PWM_OFF}	VSLV operating current (PWM not switching)	500	mA	
VSHV	High-voltage power supply	340	V	
Fly_PWM	Driver isolated power supply freq	~260	kHz	
HV_GD_VCC	Driver isolated positive power supply voltage range	18	V	
HV_GD_VEE	Driver isolated negative power supply voltage range	-8	V	
PWM_DEAD	Dead time	≅ 3	μs	
HV_OV	Over voltage protection	420	V	
HV_UV	Under voltage protection	250	V	
IGBT_OT	Over temp protection	135	°C	
IGBT_OC	Over current protection	1500	Arms	
IGBT_DESAT	Desat protection	9	V	
Motor_max_speed	Motor Over Speed	10000	rpm	

8 Platform and Accessory Ordering Information

Table 4. Ordering information

Identifier	Name	Description
Available here	EV Power Inverter Control Reference Platform	Reference design hardware kit including: 1. MCU control board, 2. IGBT driver board, 3. Sensor board, 4. Interface board 5. Software Package
Available here	EV Power Inverter Control Reference Platform Quick Start Guide	High level guide outlining how to assemble and set up operation of the inverter reference platform kit
UM11298 (here)	EV-Inverter Enablement Kit User Guide	Detailed guide for assembling, setting up and operating the inverter reference platform kit
AN13091 (here)	Inverter Platform Design Guide Application Note	Description of the inverter platform system architecture, design, and operating characteristics
Available with purchase of kit	Platform Hardware Design Package	Schematics, BOM list, Layout of the inverter reference platform
Available with purchase of kit	Inverter Reference Platform Software Package	Platform software components: 1. Basic SW w/ Service Layer & drivers 2. Platform Software Development Kit 3. Basic Motor Demo application SW (binary) 4. Inverter GUI (Requires Python)
—	Inverter Safety SW Library & Safe State Mgr. SW	Available in third quarter 2021
UM11552 (here)	PIM SiC Software User Manual	Platform software architecture and functional operation overview
Available with purchase of kit	Platform Safety Overview	High level overview of platform Safety solution
—	Safety Design Guide Application Note	NDA Safety pack (Available in third quarter 2021)
Available here	Inverter Prototype System Test Results	Test summary of Vepco Inverter Prototype
Available here	Traction Motor Power Inverter System Evaluation Prototype	Inverter prototype implementation using NXP Reference Platform (Available from Vepco)
—	Platform Components	Refer to respective component data sheets

9 References

Following are URLs where you can obtain information on related NXP products and application solutions:

Table 5.

NXP.com support pages	Description	URL
EV Power Inverter Control Reference Platform	Tool summary page	https://www.nxp.com/design/designs/ev-power-inverter-control-reference-platform:RDPWRINVERTER
GD3100	Product summary page	http://www.nxp.com/GD3100
MC5775E	Product summary page	https://www.nxp.com/products/processors-and-microcontrollers/power-architecture/mpc55xx-5xxx-mcus/ultra-reliable-mpc57xx-mcus/mpc5775b-and-mpc5775e-microcontrollers-for-battery-management-systems-bms-and-inverter-applications:MPC5775B-E
FS6523	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/grade-1-and-grade-0-safety-power-system-basis-chip-with-can-flexible-data-transceiver:FS6500
TJA1051	Product summary page	https://www.nxp.com/products/interfaces/can-transceivers/can-with-flexible-data-rate/high-speed-can-transceiver:TJA1051
Fuji M653	Product summary page	https://www.fujielectric.com/products/semiconductor/model/igbt/ev_hev_module.html
Vepco Technologies	Website	http://www.vepcotech.com/

10 Revision History

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
AN13091 v.1	20210319	EV Traction Motor Power Inverter Control Reference Platform	NA	NA
Modifications	Initial release			

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