NXP Semiconductors
Application Note

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Differences Between S32K11x and S32K142

by: NXP Semiconductors

Contents

1 Introduction

This application note shows the differences between S32K11x and S32K142 to facilitate code migrations and focuses on the differences/considerations the users must keep in mind to make applications compatible in both Microcontroller Units (MCUs).

Although both MCUs have different cores, the two share many modules in common with some differences that are reviewed through the sections.

2 Overview

The S32K11x is the predecessor of the S32K142. The main difference between the two chips is that the S32K11x contains a Cortex-M0®+ and the S32K142 includes a Cortex-M4F®. S32K11x has smaller memory options than S32K142.

The two chips have a 64QFP and 48QFP packages option, so this makes both chips to be pin to pin compatible and facilitates the code migration process.

3 Programming and debug

The Integrated Development Environment (IDEs) such as S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach and iSystems can be used to program and debug the two chips. S32K142 supports JTAG and SWD protocols while S32K11x only supports SWD.

4 Core and system differences

The S32K11x contains a Cortex-M0+ with a Von Neumann architecture and the S32K142 contains a Cortex-M4F with a Harvard architecture as all the S32K14x chips. The Cortex-M0+ implements a binary compatible subset of the instruction set and features provided by the Cortex-M4F. The software can be moved, including system level software from the Cortex-M0+ to the Cortex-M4F. The difference in the core involves important changes in the interrupt map, the architecture between core and memories, and some features that are shown in the following table:

Table 1. Core and system differences

Feature	S32K116	S32K118	S32K142
Core	Cortex-M0+		Cortex-M4F

Table continues on the next page...

Table 1. Core and system differences (continued)

Feature	S32K116	S32K118	S32K142
Bus clock frequency	Up to 48MHz		Up to 112 MHz
System clock generator (SCG)	OSC,FIRC, SIRC		OSC,FIRC, SIRC, PLL
IEE-754 FBU	Not available		Available
IOPORT	Available		Not available
HSRUN mode	Not available		Available
External Watchdog Monitor(EWM)	Not available		Available, with external monitor pin
FIRC Clock Moni tor Unit	Available		Not available
Hardware watchdog	Available		Available
Digital Signal Processor (DSP)	Not available		Available
Instruction set	ARMv-6 Thumb Instruction set		ARMv-7 Thumb Instruction set
System Interface	Single 32-bit AMB A-3 AHB-Lite system interface		Advanced AHB-Li t e system interface
Floating-Point Unit	Not available		Available
Serial Wire Viewer (SWV)	Not available		Available
Trace	Memory Trace Buffer (MTB) (1K)		TracePort Interface Unit (TPIU)
Number of I/Os	Up to 43	Up to 58	Up to 89

The following table shows the Cortex-M0+ and Cortex-M4F block diagrams:

Table 2. Block Diagrams

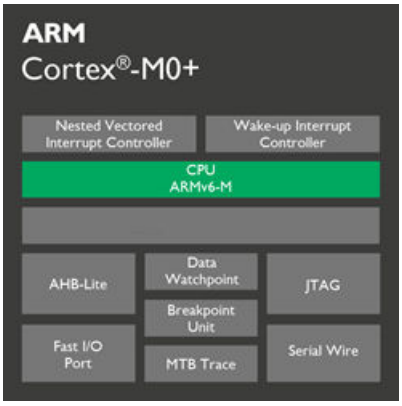


Figure 1. Cortex-M0+ Block Diagram

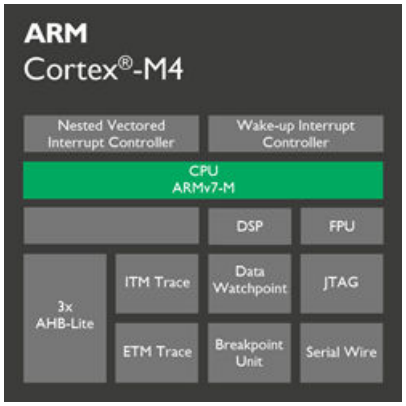


Figure 2. Cortex-M4F Block Diagram

4.1 Core and system considerations

The Memory Protection Unit (MPU) is not included in the core. In these two MCUs, this module is external to the Cores.

5 Memory

The S32K11x and S32K142 share the same memory type, but have different sizes in the P-Flash, D-Flash and FlexRAM as shown in the Table 3. The memory structure changes from the S32K142 to S32K11x. The communication between CPU and the memories is different. For S32K11x, the SRAM_L is used to store the MTB, but it can be used as SRAM without ECC protection.

Table 3. Memory size

Chip	P-Flash	SRAM	ECC Protection	FlexRAM	D-Flash	Cache
S32K116	128 KB	15 KB	SRAM_U, PFlash and DFlash	2 KB	32 KB	Not available
S32K118	256 KB	23 KB	SRAM_U, PFlash and DFlash	2 KB	32 KB	Not available
S32K142	256 KB	28 KB	SRAM_U, SRAM_L, PFlash and DFlash	4 KB	64 KB	4 KB

5.1 Internal connections

The communication of the Core with the different types of memory changes between the S32K142 and the S32K11x. As the S32K11x has the memory trace buffer feature, the Core has a direct connection to the SRAM_L which is used to the MTB.

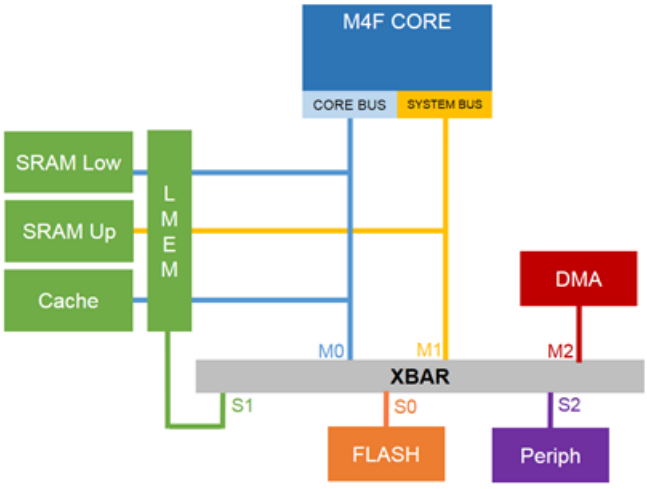


Figure 3. S32K142 internal connections of memory

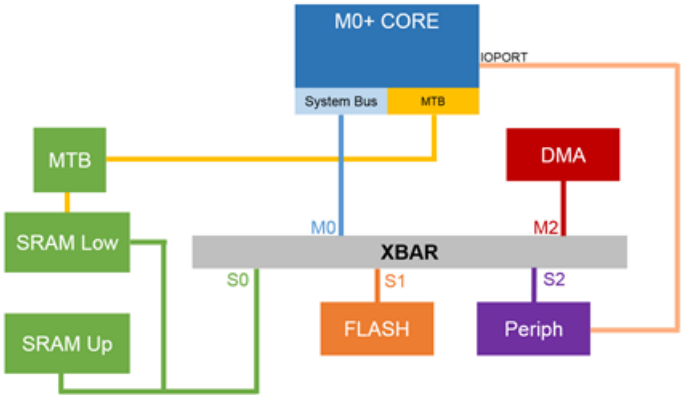


Figure 4. S32K11x internal connections of memory

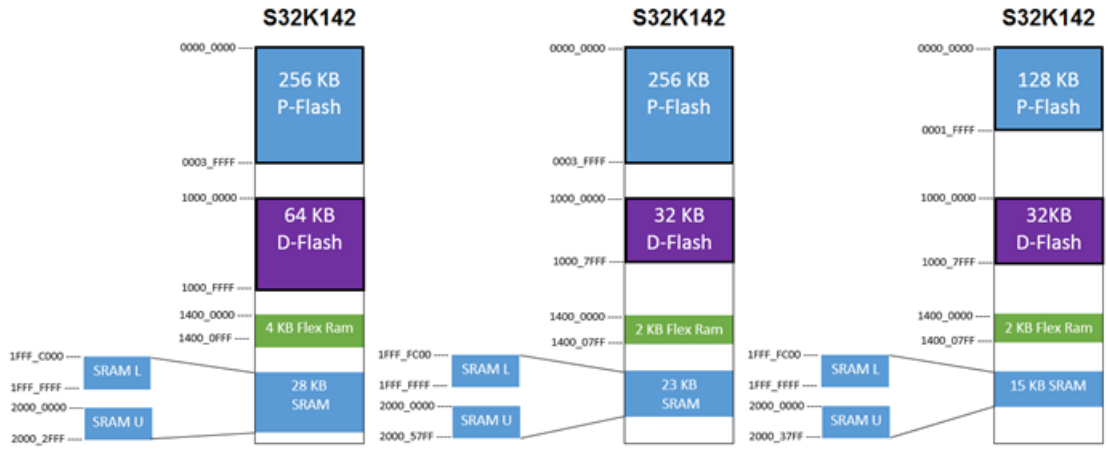
5.2 Memory address

As the memory size has changed, the start and the end of the address of each type of memory has changed as well. The Table 4 shows the start/end of the address of each type of memory.

Memory Type		S32K116	S32K118	S32K142
P-Flash	**Start Address**	0000_0000	0000_0000	0000_0000
	End Address	0001_FFFF	0003_FFFF	0003_FFFF
SRAM L	**Start Address**	1FFF_FC00	1FFF_FC00	1FFF_C000
	End Address	1FFF_FFFF	1FFF_FFFF	1FFF_FFFF
SRAM U	**Start Address**	2000_0000	2000_0000	2000_0000
	End Address	2000_37FF	2000_57FF	2000_2FFF
D-Flash	**Start Address**	1000_0000	1000_0000	1000_0000
	End Address	1000_7FFF	1000_7FFF	1000_FFFF
FlexRAM	**Start Address**	1400_0000	1400_0000	1400_0000
	End Address	1400_07FF	1400_07FF	1400_0FFF
CSE_PRAM	**Start Address**	1400_0800	1400_0800	1400_1000
	End Address	1400_087F	1400_087F	1400_107F

The following image illustrates the differences in memory of these three MCUs. In S32K11x, the SRAM_Low is used to store the MTB so the whole SRAM size is placed in the SRAM_Upper.

Figure 5. S32K142 internal connections of memory



6 Peripherals

The peripherals have the same features and functionality, the difference is the number of instances per module are reflected in the following table.

Table 4. Peripherals

Modules	S32K116	S32K118	S32K142
FlexCAN (CAN-FD ISO/CD 1 1898-1)	1 (CAN-FD supported)		2 (1x CAN-FD supported)
FlexTimer (16-bit counter) 8 channels	2x		4x
Programmable Delay Block (PDB)	1x		2x
1 2-bit SAR ADC (1 MSPS each)	1x (13)	1x (16)	2x (16)
Low-power SPI	1x	2x	2x

6.1 Peripherals considerations

- DMA for S32K11x only supports 4 channels while DMA for S32K142 supports 16.
  - For S32K11x variants, when executing a large, zero wait-stated memory-to-memory transfer, insert bandwidth control using the TCD_CSR[BWC] bit to avoid:
    - Starvation of another master accessing the memory,
    - Any delay un writing a TCD during the transfer.
- In the S32K116 and S32K118 the PTB13 does not have the ADC functionality. The ADC for S32K116 only supports 13 channels per instance while S32K118 and S32K142 support 16 channels perinstance.
- FIRCclockmonitoraddedduetoremovalofPLL.SinceFIRCisthemain system clocksource,ithasaCMUtomonitor the loss of clock.
- FIRCclockmonitoraddedduetoremovalofPLL.SinceFIRCisthemain system clocksource,ithasaCMUtomonitor the loss of clock.

7 Interrupt map

The ways in the interrupts are handled in both chips involve important differences that come from the number of vectorssupported on both Cores. The Cortex-M4F contained in the S32K142 supports 162 interrupts vectors while the Cortex-M0+ only supports 47, therefore, the interrupt vectors are allocated differently for each peripheral in both devices. For more details, refer to the interrupt map file attached in the RM.

8 Software consideration when migrating between S32K142 and S32K11x

The following considerations are needed to migrate an application from S32K142 to S32K11x:

- As a first consideration is to keep in mind that the frequency ranges are different in both MCUs; therefore, make sure your application runs properly in the S32K11x frequencies.
- Review if the size of the memory in the S32K11x is enough for your application.
- Reorganize the interrupt callbacks occurring due to the different interrupt vectors.
- In S32K11x, to disable FIRC or SIRC the user must disable the CMU, and then disable FIRC or SIRC.
- In S32K11x, the float point is not supported.
- The S32K11x does not have ECC on SRAM_L.
- Keep in mind the Core and system considerations on page 3 and Peripherals considerations on page 5.

9 Revision history

Rev. No.	Date	Substantive Change(s)
0	June 2017	Initial version.
1	August 2017	Updated the following sections: 1. Overview on page 1 2. Core and system differences on page 1 3. Memory address on page 4 4. Peripherals on page 5
2	March 2018	Updated the following sections: 1. Core and system differences on page 1 2. Peripherals on page 5 3. Memory address on page 4 4. Interrupt map on page 6
3	July 2018	Updated Peripherals considerations on page 5.

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