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Migration guide CLRC663 to derivates

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Application note
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Document information

Info	Content
Keywords	CLRC663, MFRC631, MFRC630 and SLRC610, Software migration guide
Abstract	This document describes the principles of migrating from contactless reader IC CLRC663 to MFRC631, MFRC630 or SLRC610. A practical example is given to migrate from CLRC663 to SLRC610.

Revision history

Rev	Date	Description
1.0	20120903	First release

Contact information

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1. Introduction

1.1 Scope

The main target of this document is focused on explaining the steps to migrate from CLRC663 to MFRC631, MFRC630 or SLRC610. This document will give a short overview about the changes in soft and hardware

Protocol related communication to MIFARE cards is not scope of this document. For more information on card commands and how they are used, refer to the Example Project source code, the “NXP Reader library” document and the MIFARE application notes.

1.2 Audience

This document is intended for use by manufacturers wanting to migrate from CLRC663 to MFRC631, MFRC630 or SLRC610.

2. Hardware migration

From a hardware point of view nothing has to be changed. The MFRC631, MFRC630 and SLRC610 are fully pin compatible to CLRC663. The antenna matching also doesn't need to be changed. But be aware tuning and measurement of the reader antenna has always to be performed at the final mounting position to consider all parasitic effects, e.g. metal influence on quality factor, inductance and additional capacitance.

3. Software migration

3.1 General aspects

The CLRC663 device is designed to communicate in the following operation modes:

1. read/write mode supporting ISO/IEC 14443A/MIFARE
2. read/write mode supporting ISO/IEC 14443B
3. read/write mode supporting FeliCa scheme
4. read/write mode supporting ISO/IEC 15693
5. read/write mode supporting ICODE EPC UID/ EPC OTP
6. read/write mode supporting ISO/IEC 18000-3 Mode 3

The MFRC631 device is designed to communicate in the following operation modes:

1. read/write mode supporting ISO/IEC 14443A/MIFARE
2. read/write mode supporting ISO/IEC 14443B

The MFRC630 device is designed to communicate in the following operation modes:

1. read/write mode supporting ISO/IEC 14443A/MIFARE

The SLRC610 device is designed to communicate in the following operation modes:

1. read/write mode supporting ISO/IEC 15693
2. read/write mode supporting ICODE EPC UID/ EPC OTP
3. read/write mode supporting ISO/IEC 18000-3 Mode 3

The communication distance is dependent on different factors including primarily

- the reader and card antenna size
- antenna area
- coupling between antennas
- generated Reader HF field
- minimum H-Field required by card
- environmental influences and other aspects.

To setup the main protocol settings for MFRC631, MFRC630 or SLRC610 the "loadprotocol" must be used.

3.2 MFRC631 and MFRC630

For MFRC631 and MFRC630 the supported protocol numbers stay the same. So for both derivates the "PHHAL_HW_RC663_RXTX_xxx" table, in the phhalHw_Rc663_Int.h file doesn't need to be changed.

3.3 SLRC610

For SLRC610 the protocol numbers have changed. So for both derivates the "PHHAL_HW_RC663_RXTX_xxx" table, in the phhalHw_Rc663_Int.h file, need to be changed. This can be done as shown in the example below. Added to that a "RC610_specific" flag needs to be defined in the project.

PHHAL_HW_RC663_RXTX_xxx example for using SLRC610:

```
/*@}*/

/** \name RXTX settings for #PHHAL_HW_RC663_CMD_LOADPROTOCOL
*/
/*@{*/
#define PHHAL_HW_RC663_RXTX_I14443A_106     0x00U   /**<
ISO14443A Operating mode at 106kbit/s. */
#define PHHAL_HW_RC663_RXTX_I14443A_212     0x01U   /**<
ISO14443A Operating mode at 212kbit/s. */
#define PHHAL_HW_RC663_RXTX_I14443A_424     0x02U   /**<
ISO14443A Operating mode at 414kbit/s. */
```

```
#define PHHAL_HW_RC663_RXTX_I14443A_848      0x03U   /**<
ISO14443A Operating mode at 848kbit/s. */

#define PHHAL_HW_RC663_RXTX_I14443B_106      0x04U   /**<
ISO14443B Operating mode at 106kbit/s. */
#define PHHAL_HW_RC663_RXTX_I14443B_212      0x05U   /**<
ISO14443B Operating mode at 212kbit/s. */
#define PHHAL_HW_RC663_RXTX_I14443B_424      0x06U   /**<
ISO14443B Operating mode at 414kbit/s. */
#define PHHAL_HW_RC663_RXTX_I14443B_848      0x07U   /**<
ISO14443B Operating mode at 848kbit/s. */

#define PHHAL_HW_RC663_RXTX_FELICA_212       0x08U   /**< FeliCa
Operating mode at 212kbit/s. */
#define PHHAL_HW_RC663_RXTX_FELICA_424       0x09U   /**< FeliCa
Operating mode at 424kbit/s. */

#ifndef RC610_specific
#define PHHAL_HW_RC663_RXTX_I15693_1OO4         0x0AU   /**<
ISO15693 One-Out-Of-Four Operating mode. */
#define PHHAL_HW_RC663_RXTX_I15693_HIGH_SSC     0x0AU   /**<
ISO15693 High-Speed (RX) Operating mode (Single Subcarrier). */
#define PHHAL_HW_RC663_RXTX_I15693_FAST         0x0BU   /**<
ISO15693 Fast-Speed (RX) Operating mode (Single Subcarrier). */
#define PHHAL_HW_RC663_RXTX_I15693_1OO256       0x0CU   /**<
ISO15693 One-Out-Of-256 Operating mode. */
#define PHHAL_HW_RC663_RXTX_I15693_HIGH_DSC     0x0CU   /**<
ISO15693 High-Speed (RX) Operating mode (Dual Subcarrier). */
#define PHHAL_HW_RC663_RXTX_EPC_UID             0x0DU   /**< ICode
EPC/UID. */
#define PHHAL_HW_RC663_RXTX_I18000P3M3_DS_M2    0x0EU   /**< ICode
ISO18000-3 Mode3 424 kBit/s (M=2). */
#else
#define PHHAL_HW_RC663_RXTX_I15693_1OO4         0x00U   /**<
ISO15693 One-Out-Of-Four Operating mode. */
#define PHHAL_HW_RC663_RXTX_I15693_HIGH_SSC     0x00U   /**<
ISO15693 High-Speed (RX) Operating mode (Single Subcarrier). */
#define PHHAL_HW_RC663_RXTX_I15693_FAST         0x01U   /**<
ISO15693 Fast-Speed (RX) Operating mode (Single Subcarrier). */
#define PHHAL_HW_RC663_RXTX_I15693_1OO256       0x02U   /**<
ISO15693 One-Out-Of-256 Operating mode. */
#define PHHAL_HW_RC663_RXTX_I15693_HIGH_DSC     0x02U   /**<
ISO15693 High-Speed (RX) Operating mode (Dual Subcarrier). */
#define PHHAL_HW_RC663_RXTX_EPC_UID             0x03U   /**< ICode
EPC/UID. */
#define PHHAL_HW_RC663_RXTX_I18000P3M3_DS_M2    0x04U   /**< ICode
ISO18000-3 Mode3 424 kBit/s (M=2). */
#endif

#define PHHAL_HW_RC663_RXTX_I18000P3M3_DS_M4     0x0FU   /**<
ICode ISO18000-3 Mode3 424 kBit/s (M=4). */
#define PHHAL_HW_RC663_RXTX_I18000P3M3_QS_M2     0x10U   /**<
ICode ISO18000-3 Mode3 848 kBit/s (M=2). */
#define PHHAL_HW_RC663_RXTX_I18000P3M3_QS_M4     0x11U   /**<
ICode ISO18000-3 Mode3 848 kBit/s (M=4). */
/*@}*/
```

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RATP/Innovatron Technology

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